

JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"



DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES EC8351 – ELECTRONIC CIRCUITS 1 (Regulation 2017)

Year/Semester: II/03 2021 – 2022

Prepared by Ms.S.SUREKHA Assistant Professor/ECE

SYLLABUS

EC8351

ELECTRONIC CIRCUITS 1

LTPC 3003

OBJECTIVES:

- To understand the methods of biasing transistors
- To design and analyze single stage and multistage amplifier circuits
- To analyze the frequency response of small signal amplifiers
- To design and analyze the regulated DC power supplies.
- To troubleshoot and fault analysis of power supplies

UNIT I BIASING OF DISCRETE BJT, JFET AND MOSFET

BJT-Need for biasing — DC Load Line and Bias Point — DC analysis of Transistor circuits — Various biasing methods of BJT — Bias Circuit Design — Thermal stability — Stability factors — Bias compensation techniques using Diode, thermistor and sensistor — Biasing BJT Switching Circuits- JFET — DC Load Line and Bias Point — Various biasing methods of JFET — JFET Bias Circuit Design — MOSFET Biasing — Biasing FET Switching Circuits.

UNIT II BJT AMPLIFIERS

Small Signal Hybrid p equivalent circuit of BJT — Early effect — Analysis of CE, CC and CB amplifiers using Hybrid p equivalent circuits — AC Load Line Analysis- Darlington Amplifier — Bootstrap technique — Cascade, Cascode configurations — Differential amplifier, Basic BJT differential pair — Small signal analysis and CMRR.

UNIT III SINGLE STAGE FET, MOSFET AMPLIFIERS

Small Signal Hybrid p equivalent circuit of FET and MOSFET — Analysis of CS, CD and CG amplifiers using Hybrid p equivalent circuits — Basic FET differential pair- BiCMOS circuits.

UNIT IV FREQUENCY RESPONSE OF AMPLIFIERS

Amplifier frequency response — Frequency response of transistor amplifiers with circuit capacitors — BJT frequency response — short circuit current gain — cut off frequency — fa, fß and unity gain bandwidth — Miller effect — frequency response of FET — High frequency analysis of CE and MOSFET CS amplifier — Transistor Switching Times.

UNIT V POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

Linear mode power supply — Rectifiers — Filters — Half-Wave Rectifier Power Supply — Full- Wave Rectifier Power Supply — Voltage regulators: Voltage regulation — Linear series, shunt and switching Voltage Regulators — Over voltage protection — BJT and MOSFET — Switched mode power supply (SMPS) — Power Supply Performance and Testing — Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

TOTAL: 45 PERIODS

OUTCOMES:

After studying this course, the student should be able to:

 $\bullet Acquire knowledge of <math display="inline">\clubsuit Working principles, characteristics and applications of BJT and$

FET & Frequency response characteristics of BJT and FET amplifiers

•Analyze the performance of small signal BJT and FET amplifiers - single stage and multi stage amplifiers

•Apply the knowledge gained in the design of Electronic circuits

TEXT BOOKS:

1. Donald. A. Neamen, Electronic Circuits Analysis and Design, 3rd Edition, Mc Graw Hill Education (India) Private Ltd., 2010. (Unit I-IV)

2. Robert L. Boylestad and Louis Nasheresky, —Electronic Devices and Circuit Theoryl, 11thEdition, Pearson Education, 2013. (Unit V)

REFERENCES

1. Millman J, Halkias.C.and Sathyabrada Jit, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2015.

2. Salivahanan and N. Suresh Kumar, Electronic Devices and Circuits, 4th Edition, , Mc Graw Hill Education (India) Private Ltd., 2017.

3. Floyd, Electronic Devices, Ninth Edition, Pearson Education, 2012.

4. David A. Bell, Electronic Devices & Circuits, 5th Edition, Oxford University Press, 2008.

5. Anwar A. Khan and Kanchan K. Dey, A First Course on Electronics, PHI, 2006.

6. Rashid M, Microelectronics Circuits, Thomson Learning, 2007

UNIT- V POWER SUPPLIES & Half Wlaye Rectifier: - ELECTRONIC DEVICE TESTING (3) Introduction: - This Rectifier Circuit Consists of Resistive load, Sectifying element. (i,e) p-N Junction diode and source of a.c Voltage, all connected in Series. To obtain the desided dec Rollage arross the Load a.c. voltage is applied to Rectifier Ciscuit using svitable step-up (or) step-down Fansformer. e= Esm Sinwt, w= 271f. Naturne Ratio: - No = Esm ESM, Pm + Peak Value of Secondary & primary a.c. Voltage. EID ZRL AN ABILE CKE SRL Ede= ON Fig(b): Revense Biased. tig (a): Foonland Blased -ve Half cycle. Operation: - the Half cycle A is -ve with B A Becomestive with B Diode - Reverse Brased Drode-Forward Brased Current - No current flows. Current - Clockwise disection OFF GOPTION DA. NO / OFF PS 211 ÎL wt CL >wt Voltage algoss 7411 377 2111 11 > wt diode Peak Value of Load current is given by, Im = Esm Rf+RL+RS RL -> Resistance of Secondary winding of transferrie RS -> forward Resistance of dioder dioder

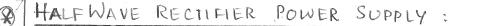
(1) <u>Average</u> (or) d.c. Value of Load current (IDC):-NL= Imsinut, o≤wt≤ II, Poc = EDC. IDC =) IDCRL 1/= 0 , AS where 211 POCE IOC RL = [Im] RL $/IDC = \frac{1}{2\pi} \int^{2\pi} i d(wt)$ $= \underline{\operatorname{Im}}^{2} \cdot \operatorname{RL} = \underline{\operatorname{Im}}^{2} \cdot \operatorname{RL}$ $\overline{\operatorname{II}}^{2} \cdot \operatorname{RL}$ $\overline{\operatorname{II}}^{2} \cdot \operatorname{RL}$ $= \frac{1}{2\pi} \left[2\pi \operatorname{Im} \operatorname{Sin}(wt) d(wt) \right]$ PDC = ESm RL As No current flows during TT RF + RL + RS 2 -ve Half cycle. (i,e) wt=TI to 21 (V) A.C. power Input (Pac)-IDC = 1 In In Sin wt. dwt. PAC = ZRMS [RL+ Rf+ RS] $= \frac{I_{m}}{2\pi} \left[-\cos \omega t \right]_{n}^{T}$ IRMS = IM $PAC = \frac{Im}{RL + Rf + Rs}$ $\overline{Loc} = \underline{Pm}\left(-\left[-1-1\right]\right)$ (M) <u>Rectifier</u> Efficiency: -- Ipc = Im EDC=IDC·RL=JIm. RL $= \frac{\prod_{m=1}^{2} RL}{\prod_{m=1}^{2} RL} = \frac{4}{\prod_{m=1}^{2} RL}$ $EDC = \frac{ESm}{(R_f + R_L + R_S)II} + R_L$ Ins [Rf+RL+Rs] (Rf+RL+Rs) = RL => y= 0.406 - EDC = ESM (RS, Rp -> Small) Neglected $1 + \left(\frac{R_{f} + R_{s}}{R_{1}}\right)$ Iliy RMs Value of Load Current 1. Imax = 0.406×100 => 40.6%. (IRMG):-(-: Rf + RS << RL) $\frac{1}{2RMS} = \sqrt{\frac{1}{2\pi}} \int_{0}^{2\pi} (ImSinut)^{e} d\omega t$ (Vii) <u>Ripple Factos :-</u> Output of the thrave sectifier = $Im \sqrt{\frac{1}{2\pi}} \int_{0}^{\pi} (1 - \cos 2\omega t) d\omega t$ is not pure dic but prisating d.c. The ortput contains Pulsating Components Called $= Im \sqrt{\frac{1}{2\pi}} \left[\frac{\omega t}{2} - \frac{3in2\omega t}{4} \right]^{1}$ sipples. $= \mathbb{Z}_{m} \sqrt{\frac{1}{2\pi} \left(\frac{\pi}{2}\right)} = \mathbb{Z}_{m} \dots \mathbb{S}_{m} (2\pi)$ The Measure of ripples present is the output is with the help = Sin(o) = o of a factor called sipple Irms = Im EL(RMS) = Inns RL factor; denoted by y'. Smaller the Apple factor closer EL(RMS) = FSm/2 in D.C. power output (Ppe):is the output to a puredic.

Ripple factors It is defined ZESM XRL 6 as the Ratio of R.M.s Value of TI RF + Rs + R2 the a.c. Component in the overput $% R = \frac{E_{Sm}}{TT} - \frac{E_{Sm}}{TT} \frac{R_2}{(R_F + R_S + R_2)}$ to the Average or d.c Component present in the output. ESTO REL TI RE+RS+RL Y = R.M.S. Value of a.c. Component Ripple of output => 1- RL × 160 factor Average (or) d.c component of output RF+RS+RL RL Imms = VIac+Idc RFFRSTRL % = R<u>F+RS X100.</u> Iac = V Imms - Ide (X) Transformer Utilization factor Y = <u>Lac</u> =) VInns-Ide Ide Ipe (T.U.F) :-T-V.F= D.C power devilered $\gamma = \sqrt{I_{ms}}^2 - 1$ Idc to the Load A.C. Powers rating of the $Y = \sqrt{\left(\frac{2}{2}\right)^2 - 1} = \sqrt{\frac{1}{2}} - 1$ transformer Pole = IDE RL =) (Im) RL. $\left(\frac{2m}{T}\right)$ Y is Very High. 7 1.2) A.c power rating of Fransformer. vili) peak Inverse Voltage (PIV) = Erms · Loms =) <u>Egm. Im = Almla</u> Va. Va. 2 It is the peak voltage $T \cdot U \cdot F = \frac{Im^2}{RT^2} \cdot \frac{R_L \cdot 2\sqrt{2}}{2m^2 R_L} = \frac{2\sqrt{2}}{T^2}$ across the diode in the reverse direction (ie) When the diode T. U.F= 0.287 is genease brased. This is Called PIV Rating of a drode. (XI) Advantages:a) only one dide is sufficien PIV of diode = Esm for Half Wave rectifier b) CKF is easy to design c) No centre tap on transformer (X) Noltage Regulation:-& Necessary % Voltage Régulation = (XII) DisAdvantages! a) Ripple factor of HWR CKE (Ide) NL - (Vde) FL X100. is 1.21, which is thigh b) Max. rectification efficiency (Vdc) FL is for , which is low (Vdc) NL = ESM/T 0) T. U. E is low Showing Hat transformer ingering NEUlly Utilise (Vac) FL = IDC. RL = Im. RL

UI FULL WAVE RECTIFIER !-Fig: Inlaveforms. Introduction: - It conducts Esm during both positive and 0 Negative Maif cycles of idi inputa.c. input, two diodes aste used in this circuit. The diodes feed a common Load RL with the help of a 1d2 Centre tap transformer. The A.c. Voltage is applied through al Svitable power transformer 15 with proper turns rateo. Opegation: - (tre) Half cycle 011 A is the W. B is - Ve (undret) Diode D, -> forward blased (Not conduct Diode D2 -> Reverse Blased () Maximum Load current:-Open CKts .. Im = KSm (-ve) daif cycle. RS + RF + RL A' is-ve N. B is + Ne. Rf -> formand Resistance (Conduct) Diode D2->-forware Biased Rs - Winding Resistance Not conduct Diode DI > Reverse Blased Im -> Maximum Load current Esm -> Max. Value of a. c i/p Voltage "Load current-flows in both the Half cycles of ac stoltage of secondary (1) D.C. Load current and in the Same direction Em Sinut through the Load Sesistance. $I_{L} = I_{m} Sin \omega t$, $O \le \omega t \le \Pi$ $lav = IDC = \frac{1}{\Pi} \int_{-\pi}^{\pi} i_{L} d(wt) =)$ = I IT Im Sin wt dut fig(full/ klave Rectifies. = Jm [-coswt] Centre tap transformer Ы $= \frac{lm}{\pi} \left[1 - (-1) \right] = \frac{2 lm}{\pi}$ The output Load current is strill pulsating d.c and (til) Average Dc Load Voltage (EDC) !-EASYENGINEERING.NE not pure d.c. EDE = LDE. RL =) 2. Im RL

) What are the						
(*)) Derive the expression for the Rectification afficiency,						
	Ripple factor, transformer Utilization factor, form factor and peak factor of Halfevalle Rectifier. (8m) F) Draw and Explain the Working of Halfware Rectifier (6m)						
	and peak fact	or of Halfeva	ve rectifies.	ave Rectifier (bm)			
िम	Deaw and Rx	plais the klos	in a trill wa	Ve Rectifier &			
CX.	1 Thou and Pr	plain the RIDAL	4 +				
	derive all the	pagameters					
Ans'.		11 Dec-02 the	r-06 May-	12, May-14]			
	[May-10, Dec-		Tell & Lasta	Bridge Rectifies			
SL.No	Parjameter	Half Iklave	full mave	and the free right			
e fillene	No. of diodes		2	T			
2 -	Ripple Frequency	50HZ	100HZ	100HZ			
3.	piv rating of diad	e ESm	a Esm	ESm			
4.	Avg D.c current		2.Im TT	2.J.m TT			
5.	Avg D.c Voltage (EDC)	ESM	2 ESm TT	a ESM TT			
6-	R.M.S current (IR	3) <u>Im</u>	Im V2	Im V2			
7.	D.c power output (Poe)	Im ² RL TT2	A Im RL TT2 Im RL	$\frac{4}{\pi^2} T_m^2 R_L$			
8.	TUF	0-287	0.693	0.812			
9.	A.C. power output P(Ac)	$\frac{J_{m}^{2}(R_{L}+R_{S}+R_{f})}{4}$	$\frac{J_m(R_f \rightarrow R_S + R_L)}{2}$	Ino (Rg + Rg + RL) 2			
10-	Maximum rectifier efficiency (n)	40.67.	81-27.	81-27.			
	Maximum Load	ESm	ESm	Esm			
	Curgent (Im)		RS+Rf+RL	Rs+2Rf+PL			
12.	Ripple factor (2)	1.21	0.482	0.482			
gvn:-	Compare all l Wave, Half K	the parameter	is klitts the	Bridge, Full			
Ange		lave Rectifie	EASY	ENGINEERING.NE			
Ans.	[Above].						

$$\begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \mathcal{C} & \mathcal{D} & \mathcal{C} & \mathcal{C} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} \cdot \mathcal{C} & \mathcal{I} & \mathcal{D} \\ \hline \mathcal{B} & \mathcal{C} & \mathcal{I} & \mathcal{C} \\ \hline \mathcal{B} & \mathcal{C} & \mathcal{I} & \mathcal{C} & \mathcal{C} \\ \hline \mathcal{B} & \mathcal{C} & \mathcal{I} & \mathcal{C} & \mathcal{C} \\ \hline \mathcal{B} & \mathcal{C} \\ \hline \mathcal{C} & \mathcal{C} \\ \hline \mathcal{C} & \mathcal{C}$$



is CAPACITOR FILTER CIRCUIT:

→ When a sinusoidal alternating voltage is rectified, the nerulting waveform is a series of positive or negative half cycles of the input waveform, it is not direct voltage. To convert to direct voltage, a shoothening excuit or filter is needed. Reservoir

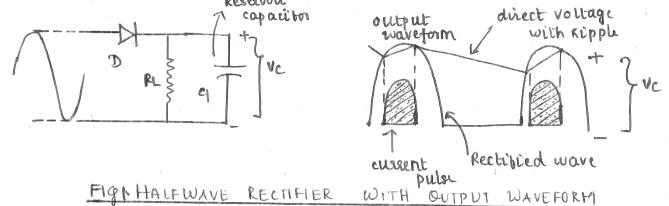


Fig. consists of a single capacitor filter (C1) and a load resistor (R1). The capacitor termed as a reservoir capacitor is charged almost to the peak level of the circuit input voltage when the diode is forward biased. This occurs at Vpi as shown in below Fig.

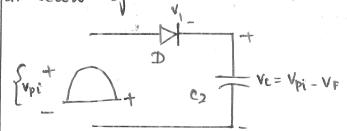


Fig. G charged to Vpi - VF

 \rightarrow The peak capacitor voltage $V_c = V_{pi} - V_F$ \rightarrow the instantaneous level of the input falls below V_{pi} the diode becomes reverse biased. The capacitor begins to discharge through the load resistor (RL) when the diode is reverse biased. So V_c falls slowly as shown by the capacitor voltage in the fig 1.

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Fig. Di is reverse bicesed when V; falls

(13)

-> The diode remains reverse biased throughout the rest of the positive half cycle. - - CURLARE flows through the didde to recharge the capacitor at this point, causing the capacitor to reach (Vpi-VF)--> The circuit output is then a direct voltage with a small Ripple waveform superimposed. RIPPLE AMPLITUDE AND CAPACITANCE: - The amplitude of the nipple voltage is abjected by three parameters. such as reservoir capacitor value, load current and capacitor discharge time, -> The discharge time depends upon the greatency of ripple waveform. - with a constant load current, the nipple amplitude is inversely proportional to the capacitance. --- The reservoir capacitor value can be calculated from load current ripple amplitude and the capacitor discharge time. direct Voltage with Ripple cmail) EDONY : E. Formax) Eormin) (mak) 022 IE - 180° - 90--057 900 current puls - RELATIONSHIP BIN Formax, & Earnin) CAPACITOR WAVEFORM AMPLITUDES ANGLES & TIMES The waveform parameters are: for t1 - capacitor discharge time a) Eave = average de ojp voltage 8) to - capacitor charge time b) Eocmax, - maximum of voltage h) of - phase angle of ilp () Eocmin - minimum op voltage from oto Evenin) 7 - time period of ac ip waveform d) i) of - Phase angle of ilp e) Vr - Vipple voltage p-to -p amplitude EASYENCINEERING NE CHAY).

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RELATIONSHIP BETWEEN EDIMONS and EDIMON: Since the input wave is sinusoidal, Eocmin) = Eocmax) sino, which gives Of = sint Examin, Eormax $B_{g} = 90^{\circ} - 01$ The period, T = 1 where f = frequency of a if waveform t in degree \implies t/degree $= \frac{T}{360^{\circ}}$ $t_2 = \frac{Q_2 T}{360^{\circ}}$ and $t_1 = T - t_2$ Taking current as constant, $c = \underline{J} t$ CAPACITOR SELECTION : -) Large standard value capacitor is always selected in case of a reservoir capacitor. -> The standard value capacitors are available with ±20% tolerance. capacitors of more than 10 pF, the tolerance is -10% to + 50%. I The de working voltages can be quite small for large value capacitors. Else capacitor dielectric may breakdown. CAPACITOR POLARITY: > straight har DI DI Japut 5002 SRI + positive terminal If the capacitors are incorrectly connected, polarized capacitors explode. This have tragic conservences for the eyes

(15)

of an experimenter.

The positive terminal is represented by straight basis on the component graphic symbol. This should be connected to the positive point in the circuit. EASYENGINEERING.NE

16 APPROXIMATE CALCULATION: APPROXIMATION 1: is Assume the load current & constant. in Normally, the load current charges by small that it has no significant effect on the calculation. APPROXIMATION 2 : Discharge time (4) is approximately equal to the input waveform time period cts [t=F] DIDDE SPELIFICATION: The selected diodes must be able to survive higher levels. VR= 2Vpj ____ VR and tVp at cathode, so diode G] peak reverse voltage is VRN2VP The average forward current that a diode pass is equal to the de output current. $I_{F(0V)} = I_{L}$ The diode of a half wave rectifier with a reservoir capacitor does not conduct continuously but repeatedly passes pulses of current to recharge the capacitor each time the diode becomes forward biased. So the current pulse is known as repetitive surge current and is designated as IFRM. IFRM over time period T must be erual to IL. IL = JFRM Xt2 => JFRM = JL(t1+t2) (t_1+t_2) t, DI

SURGE LIMITING RESISTOR (RS) IN A HEASYENGINEERING.NE

Rs IF(surge)

-4

The purpose of a low resistance surge limiting resistor (Rs) connected in zeries with the diode of is to limit the level of any surge current that might pass through the diode If switch-on occurs, the ac current is,

$$I_{F}(surge) = \frac{V_{P}}{Rs}$$

$$= \frac{V_{P}}{I_{FSH}} \quad \text{when } I_{F}$$

n IFCSUrge) is maximum (IFSM)

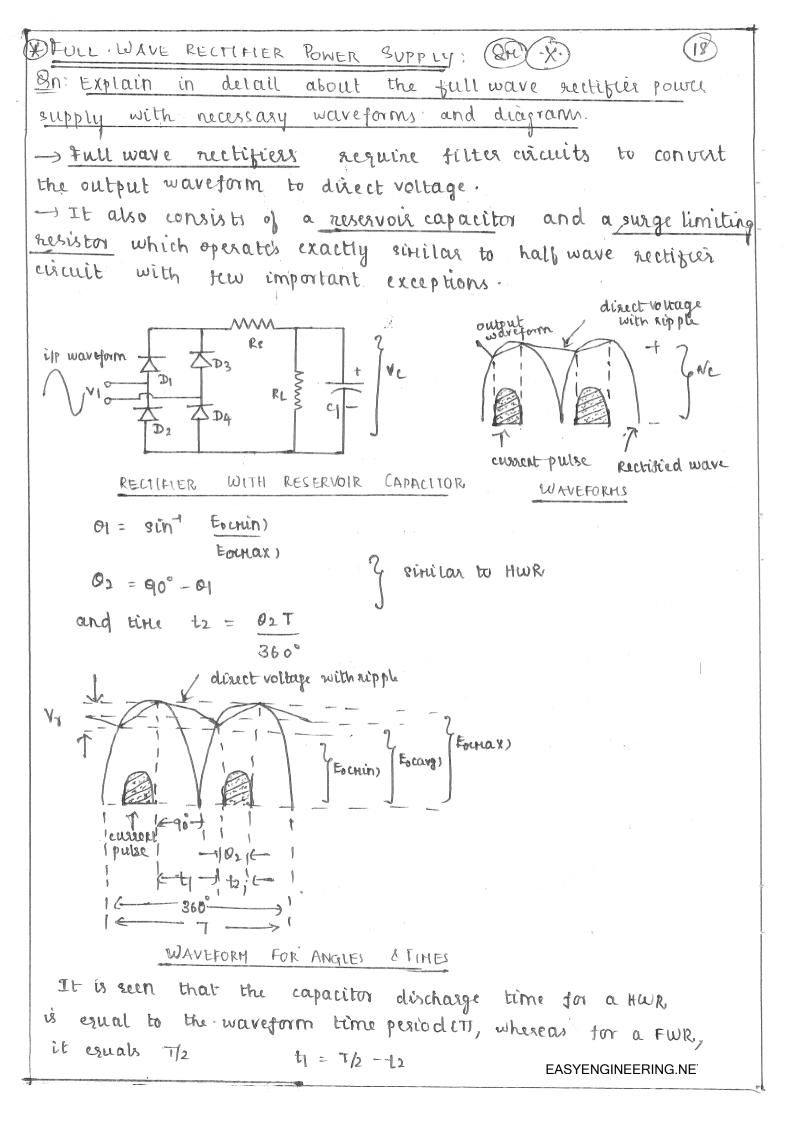
TRANSFORMER SELECTION :

A power supply transformer is normally defined in terms of rms input, and output voltage and current. The input is usually 115V, 60 Hz supply and the transformer peak output voltage is calculated by adding the rectifier Voltage drop to the power supply peak output. The peak voltage is converted into rms to give the secondary value.

VSCIMS) = 0.707 (EDIMAX) + VF) for a HWR with resistive load, Jims = 2.2 Judis. for a HWR with capacitive filter, Judes = 0.28 Jscims) =) Jscimsi = 3.6 Judes.

The transformer primary current is

Iperms) = Vscoms) × Iscomy $|(\mathcal{F})$ Vp LYMS) Sn: Give a detailed account on half wave rectifier power supply with necessary specifications and selections.



Using the wrect value of a reservoir capacitance for a full wave rectifier can be calculated from

$$C = \frac{ILH}{V_T}$$

sitularly, the repetitive current IFRM can be determined as

$$\frac{\text{IFRM}}{\text{t}_2} = \frac{\text{IL}[t_1 + t_2]}{t_2}$$

The diade average current is equal to the ball the load current.

Another dibberence between FWR and HWR power supply circuits concerns the neverse voltage applied to the diode. When the instantaneous input voltage is typ, the neverse biased voltage across D_3 is $V_R = V_P - V_F$

Revuese voltage

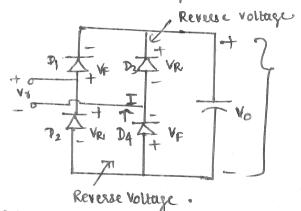


Fig .: \$10\$ REVERSE VOLTAGE FWR CIRCUIT

TRANSFORMER BELECTION:

The transformer specification for a FWR is sitular to the HWR. Two diode voltage deops involved in calculating the secondary rms voltage.

VSCOMS) = 0.707 (Eocmax, + 2 VF)

for a FWR with capacitive filters 1 ILcdcs = 0.62 Iscims) Its with all transformen, the prinary current is

Ip (TMB) = "S (TMB) x Is (TMB)

VP(rms)

	DITAGE REGULATORS:
	-> A nectifier with appropriate filter requires a good de
	power supply. The main disadvantage is that the dc output
	voltage changes with change in the input voltage or load current.
	since the de output voltage is not constant, this type of
	power supply is called unregulated power supply
	> An order to ensure a constant voltage supply negardless
	of the variations in input voltage or current, a voltage
	stabilization device called voltage regulators are used.
	-) The voltage negulator circuit keeps the output voltage
D	CONSTRUCT SOCIES IN A STRUCTURE S
Sh:	
	A voltage regulator is a device designed to keep the output
	voltage of a power supply as nearly as constant or possible.
\bigcirc	
CH CH	BLOCK SCHEMATIC OF REGULATED POWER SUPPLY.
	On Sketch and explain the block skhematic of regulated
	-> IL
	Unregulated De Vin from Voltage DL REGulated ZRL
	Stiter Regulator Vout
	The input to a voltage negulator is an unregulated de
	supply whilk the output is segulated de output voltage.
	Vout which is almost constant Primary Secondary + constant
	Transformer Rectifier DC Filter DC Regulator Shooth
	mains Voltage Pulsating type Unregulated To Load
	230V, 50Hz
	Stepdown Rectibiliz Filter Regulation de
	the states of th
а.,	
	Fig. BLOCK SCHEMATIC OF RPS WITH WASYENGINEERING.NE

$$= The transforman steps down the ac voltage cliputs, (2) to the level sequired for the devided de output:
$$= The next sequired for the devided de output:
$$= The next sequires this ac voltage into a publishing de voltage containing sipples in its:
$$= Then the stitue execute schemes the nepple content and tries to make it smoother.
$$= still then the stitue original reduces the nepple. called unsegulated de voltage.
$$= Then the negulation evoluties some nipple. called unsegulated de voltage.
$$= Then the negulation evoluties to unset the output de voltage constant: the output is called de voltage to which the load can be connected.
$$= Then the negulation evolve supply respondence of a de sasies regulation (1) or (10).
$$= The your segulation evolve the load cas the change in the negulated output voltage when the load caster changes are not intermed to a segulation = V_{NL} - V_{FL}$$

$$= Vol tage acquisition = V_{NL} - V_{FL}$$

$$= Vol tage acquisition = V_{NL} - V_{FL}$$

$$= Vol tage intermed to the stage of the segulation is a transformed of the segulation is a segulation intermed to the stage of the segulation is the segulation = V_{NL} - V_{FL}$$

$$= Vol tage acquisition = V_{NL} - V_{FL}$$

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(III) LINE REGULATION (SOURCE REGULATION) :
The line regulation can be defined as the change in
regulated load voltage for a specified range of live voltage.
Line Regulation = VIIL - VLL
VHL-High line load voltage VLL-Low Line load voltage
7. Line Regulation = VHL-VLL ×100
Vnorinal
= A Voult - 100 V
$= \frac{\Delta V_{out}}{\Delta V_{in}} \times 100 \%$
NID. OUTPUT RESISTANCE =
+ Rout H 1 when no load is connected to
- VI=Voult Spi
VM_ S COUR HOLDE VL = VNL
when when when when when when when when
Power supply Fig. concept of Rout VL = Vout = VNL - IL Rout
Practically, Rout is very small in the range of <u>milliohms</u> .
The value of Rout is obtained grom the slope of load regulation
characteristics - CREfer Load Regulation topic graph).
Rout = ΔV_{L} vin and Temperature constant
(IV) VOLTAGE STABILITY FACTOR (SV):
So is the percentage change in the output voltage
which occurs per volt change in the input line voltage with
load urrent and temperature as constant. Shaller the SV, better
$S_V = \Delta V_{out}$ ΔV_{in} IL and Temperature constant the performance of power supply.
(V) TEMPERATURE STABILITY FACTOR (ST): The temperature stability of a power supply will be
deternited by temperature coefficients of various seniconduct
devices, $T = \Delta Vout$ ΔT Vin EIL constant. This should be as small as <u>possible</u> AsyENGINEERING.NE
possible ASYENGINEERING.NE

(VI) RIPPLE REJECTION :

The output of a nectifier consists of <u>sipples</u>. So <u>sipple</u> tigetion is a factor which indicates how effectively the negulator encuit rejects the nipples and attenuates it from input to output. If VR is the nipple voltage then RR is given by

RR =	Ripple in	output	= VRCOULI
	Ripple in	înput	VR Lin)
In decibe	k, $RR' =$	20 Logio RR	dB

As vecouts is always less than vecin, RR' ie RR in dB is always <u>negative</u> when defined as vecouts/vecin).

(VII) TOTAL CHANGE IN OUTPUT VOLTAGE:

If input voltage, load current and temperature are affecting the negulator output voltage, then the total change in output voltage is $\Delta v_0 = Sv \Delta v_{in} + R_0 \Delta I_L + ST \Delta T$

DILINEAR / BASIC VOLTAGE REGULATOR:

The basic voltage regulator consists of: is Voltage reference, VR (ii) Error amplifier iii) Feedback network (ii) Active serves (on shunt control element The voltage reference generates a voltage revel which is applied to the comparator circuit, which is generally an error amplifier.

-> The second input to the error anplifier is from the feedback network:

→ The error amplifier converts the difference between the output voltage and the reference voltage into the <u>error signal</u>. → This <u>error signal</u> then converts the active element of the <u>regulator circuit</u>, in order to compensate the change in output volto → <u>Transistor</u>, is used as an active element. Thus the <u>output</u>. Voltage is <u>maintained</u> constant.

24 TYPES OF VOLTAGE REGULATORS: An: Explain with the block diagrams, the basic types of voltage regulator circuits (8H) (or) (13H) (-x) There are two types of voltage regulators available, namely, (i) series Voltage Regulator in shurt voltage Regulator 1) SERIES VOLTAGE REGULATOR: VI=Vo control Vin element Regulated Vrseg ulated control. Sanpling signal circuit Comparator Reference Feedback circuit Voltage signal HAS BLOCK DIAGRAM OF SERIES VOLTAGE REGULATOR - If in a veltage regulator cricuit, the control element is connected in series with the load, the circuit is called series voltage regulator circuit. -> The unregulated de voltage is the input to the circuit. The control element controls the amount of input voltage, then gets to the outputy" -) The campling circuit provides the necessary feedback signal. -> The comparator circuit, compares the seedback with the reference voltage to generate the appropriate control signal. -> If Vo decreases due to increased load, then error detector produces an output that causes the control element to increase Vo. -> Similarly, any tendency of Vo to increase, results in a signal that causes the control element to reduce Vo . EASYENGINEERING.NE

$$\frac{g}{Fannsetor 3eries Recention (OR) Emistre follower Series Voltage
REGULATOR:
 $\frac{g}{g} \cdot \frac{g}{g} \cdot$$$

,

2

EXPRESSION FOR VOLTAGE STABILITY FACTOR (SV):

The voltage stability factor for enitter follower reries

 $S_V = \frac{R_Z}{R + R_Z}$ where $R_Z = ac$ resistance of alynamic resistance

(26)

The value of Rz is viry chall and by selecting the Large value of resistance R, SV can be reduced. Ats ideal value is repro (0).

EXPRESSION FOR OUTPUT RESISTANCE:

The output voltage Ro can be defined as the ratio of applied voltage V to current I. For emitter follower SVR,

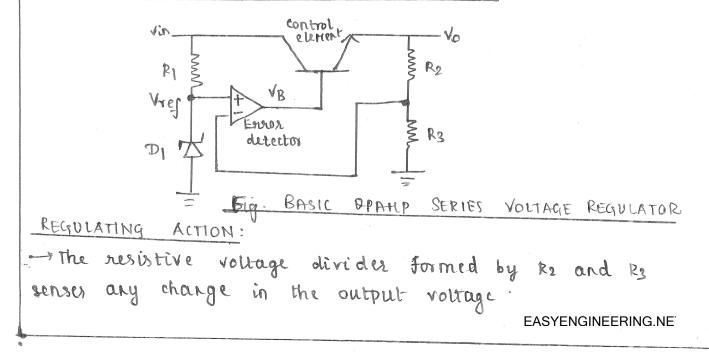
 $R_{0} = \frac{V}{I} = \frac{R_{z} + hie}{1 + hje}$

It can be reduced by selecting a transistor with high value of here.

DISADVANTAGES DE EMITTER FOLLOWER SERIES VOLTAGE REGULATOR: is The charges in VBE and Vz due to charges in temperature appear at the output '

in oue to large power dusipation, heat sink is necessary which makes the circuit bulky.

() OP-AMP BASED VOLTAGE SERIES REGULATOR:



 \rightarrow when the output tries to decrease, due to increase in ^[27] load current IL caused by a decrease in R1, a proportioned voltage decrease is applied to the op-amps investing input by the voltage divides.

across the opamp's input.

-> This difference voltage is amplified, and the opamp's output voltage VB décreases.

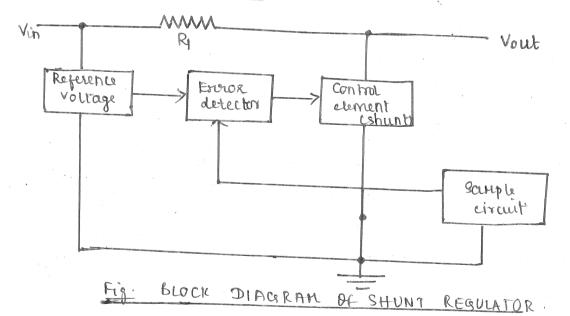
"This causes vout to increase until the voltage to the inputagain equal to the reference voltage.

The closed loop gain

5.0

$$AcL = 1 + \frac{R_2}{R_1}$$

ID SHUNT VOLLAGE REGULATOR :



->If the control element is connected in <u>parallel</u> with the load, then the regulator circuit is called <u>shunt voltage</u>

 \rightarrow The operation of the circuit is similar to that of series regulator, except that regulation is achieved by controlling the current through <u>parallel</u> transistor Q_{1} .

a) TRANSISTOR SHUNT REGULATOR:

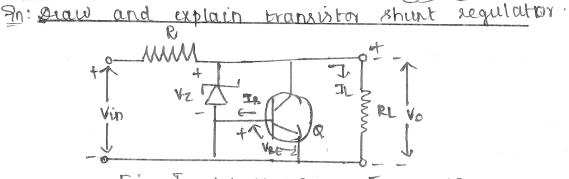


Fig. TRANSISTOR SHUNT REGULATOR, -> A <u>transistor</u> is used as a <u>control element</u> and is being connected in <u>shunt or parallel</u> with the load. -> The output or load voltage is equal to the sum of zenos voltage Vz and the base emitter voltage VBE of the transistor.

(Gr) (-3)

(28)

Vo = VZ FVBE

REGULATING ACTION:

→ Assume that the unregulated input voltage increases. Due to this, the load voltage V also increases. → As a result collector current of the transistor Ic also increases.

-I This causes the input current 'Ii to increase, which inturn increases the voltage drop across the series resistance R. consequently. load voltage decreases. -I 4t is valid because of the voltage drop across ceries resistance VR and the load voltage is equal to the input voltage, at all times.

VE = VR+VL

How diagram:

VIT -> VLT -> VBET -> IBTICT -> VRTVE

Switching Regulator: The operating painciple of switching sogulator is Completely different than that of linear regulator. Switching Segulator requises an external transistor and a choice. The Seales pass bansiston in such a regulator is used as a Contaolled switch and is operated in Cut-eff sogion (09) Saturation sogion. Hence the power beansmitted access such a bransistor is in the Josm of discrete pulses rather than a steerly flow of casent. when the bansiston is operated in the cut off region there is no custont and obssipated. no power, while when it is operated in the saturation region a regligible vollage drop appeals accoss it and hence dissipated very Small power. provided max current to load. Therepse Switching segulators uses the fact that if Cycle of the pulse variepan is varied, the average duly value of the voltage also changes propositionally. Duby cycle $\delta = \frac{ton}{t_{out} t_{out}} = \frac{ton}{T} = ton f$ Fout falt Lon - On Lime of pulse; Logy - off lime of pulse. The basic switching segulators consists of your major Components (a) Vollage Source A Switch Filler. (b) Switching Isansisboa Vin (JII) Pulse 1 generation. LOAD (c) Pulse generators & Filley. tig Basic Switchi

Switched Mode Power Supply :- (SMPS)
A power Supply is an impostant element of any
type of electronic circuit. It provides the supply for the
proper operation of circuit. The Successful operation of the cira
depends on the peoper junctioning of the power Supply. Mos of the electronic circuits requires a smooth de voltage as
that of ballesies. The power supply in a circuit traics to
paovides such a Constant Voltage.
The segulator in a power supply is an
The segulator in a power Supply is an impostant unit which keeps the output de voltage. Constant under the Veriable load and Variable input Condit
Constant under the Voriable load and Variable input circuit
Need of Switched mode power Supply:- A linear power supply has following limitations
a) The sequised input step down beanspormer is
bulky and expensive.
b) Due to low line prequency, large values of filter
Capacitos are required.
c) The efficiency is very low
d) As large is the difference between input and output
Voltage more is the power dissipation in the series
pass Lansiston.
e) The nead jost dual Supply is not economical and jeasible to achieve with the help of linear regulators.
To overcome all theese limitations SMPS are needed.

Vav -Tott-> less ton less Var. Vav Tott Mose Lon More Nav Vav Pulse width modulation. 4.9. The Switch is generally a beansistor. The pube generators output makes it on or or of the pulse generators padrices à sequised puble wavejoam. The most effective pulse waveport prequency is doktz. and lange of Commonly used gitter is RLC. the most Volkage Regulatos: -Switching voltag basic Switching The block diagram of 2 1 Segulato 9 which uses transistor a a Switch as shown in next page. working ! past R2 /R, + R3 of the output is jed The the Lo investing back input of expansion period in the comp

with the soperance voltage. The difference is amplified and given to the comparator inverting terminal. The Oscillator generates à briangular wavejorm at fixed prequency. It is applied to the non-inverting lemin of the Compagalos. The output of the Compagalos is high when the Esiangular Vallage wavejorm is above the level of the essos amplijies output. due to this the biansistas & aemains in cutoff state. Thus the output of the but a sequised pulse wave asm. Comparator is nothing Pulse Vin wavejoan amplifier 60 Oscillatos 內平 Feedback Voltage sozerence. fig. Block diagram of Switching regulator. The period of the public wavepoin is some as that of oscillators output say T. The duty cycle is denoted as 8 = Lon IT. This duty cycle is contaolled by difference between the feedback vollage and reference vollage. when or is on in saturation state, the entire input voitage vin appears at point A TEASYENGINEEBING NEWS Sharang

Inductor.

when Θ is eff, L, Still Continue to supply customate through itself to the load. The clode D, provide the setuen path jos the customat. The Capacitors C, act to smooth out the voltage and the voltage at the output is almost dc in nature. The output voltage Vo expressed mathematically as $V_{\Theta} = \frac{ton}{T}$ Vin = 8 Vin.

The sange of operating prequency to get max efficien, is to to so kHz.

Types of Switching Regulatoss: The Switch mode segulatoss use an inductor and there is no input to output isolation. On the otherhand otherside Converters use transporting and may provide input to Output isolation. These are three basic Conjigurations of switching

regulators.

1. step down (OA) Buck Switching Regulator 2. step up (OA) Boost Switching Regulator 3. Investing type switching Regulator

1. Step down Switching Regulator :- (Buck) It Consists of inductors L and series transistor & which act as a switch. The superance for error amplijier is provided by zener vollage Vz. The output is Jed back to essos amplifies through postential divider. The pulse width oscillator controls the EASTENGINEERING RE Q as

on the load sequisement. depending OS OFF ON Q o Vout. Vino Unsequested ID, Rz DC R, Vagiable pulse width Potential oscillatos. Esson ... divider. Output jeaback V2 TO Da Step down switching segulators. 4,9. The beansiston Q is used for switching the input Voltage jos the saguised pesiod of time, which is dependen on load cussont sequisement. The L-C Jilles averages the Switched Voltage. Wosking: The Variable pulse width oscillabor Controls ON LOFF pealods of Q, when on time is more composed to OFF Lim the Capacitos charges more increasing the subput voltage. on the other hand when OFF time is more compared to ON time the capacitos discharge more, reducing output voilage. Thus adjusting the duty cycle S of branststar the Vin. AD output voltage can be regulated. S= EON & FORF = Equivalent Clacuit.

а Эк - Эк

a) If output vallage decleases: The Voltage across R3 docreases. The seperance Vz is fixed. Thus eases at input of eases amplifies is more. This produces pulse of higher width as the output of the variable pulse width oscillabor. As pulse width i's high Low is higher Jor Q. This increases the charging of the apacitos C producing more output voltage. Thus decrease Output Voltage get Compensated. LON LOFA time. FON > FOLE b) when output voltage incleases: The Voltage acauss R3 incleases. The seperance Nz is fixed. The esson at the input of esson amplifier decreases. The output of the error amplifies controls the autput of vasiable pulse width oscillabos. It produces pulse of smaller width which reduces Low Jos Ob. This makes the Capacitos c to discharge more to effect any attempt of in output Voltage. increase ... The output vollage is TOFF Voul = SVin. Voul where 8 = tont EASYENGINEERING.NE

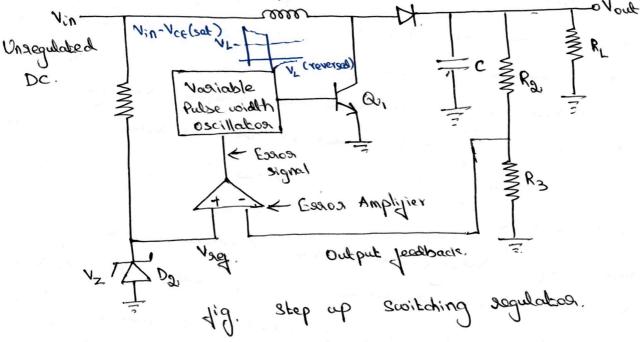
LON < FOFF

time

Ilp. Fig. Waveyoam of step down switching soundator. Nin unsegulated DC. lime Vout Vava ON Lime. Tout boad · Iav (usson ! Diode cusent Diode Disde OFF ON Lime. Adventages: 1. Higher efficiency a simple to design. 3. low supple Content-Small output filles 4. line voltage regulation. lage bolesance of S. Disaduartages: -Single output and no isolation between input and output. 1. Slow bransient sesponse composed to linear regulator. 2. 3. Due to finite reverse secondy time of Communi cabing dide the instantaneous short circuit the 220RJD occar EASYENGINEERING.NE due to which addive switches Source may

Step Up Switching Regulator: - (Boost)

The basic elements used in this type are identical to those used in step down type but their arrangement is different. L



Mosking: Case (1): when Q, is on , Vce is denoted as Vce (sat) and the Vollage acsass L suddanly become [Vin - Vcc (sat)] as shown in fig. This expands the magnetic field around the inductors very quickly. This Vollage acsocs L can be obtained by applying KVL to Vin. during on time of Q the voltage across inductors etast decreasing exponentially from its initial max value [Vin - Vcc (sat)] Case (3): when Q, is OFF. The magnetic field of the inductors L collapses and its polarity get severed. This is because an inductors current can not change instantly. Thus value of VL attacned after exponential decrease when Q, is ON now get soversed as shown in the fig. Due to soverad of polarity EASYENGINEERING.NET it gets added the Vin.

The diade D, is poward biased due to reversed V_L and Capacitor C now charge to V_{in} to V_L . The output vallag is voltage across capacitor C. which is $V_{in} + V_L$. which is more than V_{in} . Thus it adapt step up type segulator.

It can be seen that how much V_{\perp} should be added to Vin. The shostes the ON pesiod Q Q, greates voltage will get added to Vin increase the subject voltage. The longer the ON time Q Q, , Smaller is the inductor voltage V_{\perp} and loss voltage will get added to Vin, decreasing

the output Voltage. when output voltage takes to decaeases due to increase in load carsont (a) decaease in Vin itself then on time of a, get suduced thus Vin increases compensating for the decrease in it.

when output vollage tries to increase then on time of Or get increased. This reduces vollage across the inductor . Thus the lass vollage gets added to Vin, reduce its value. This compensate for the attempted increase in Output voltage.

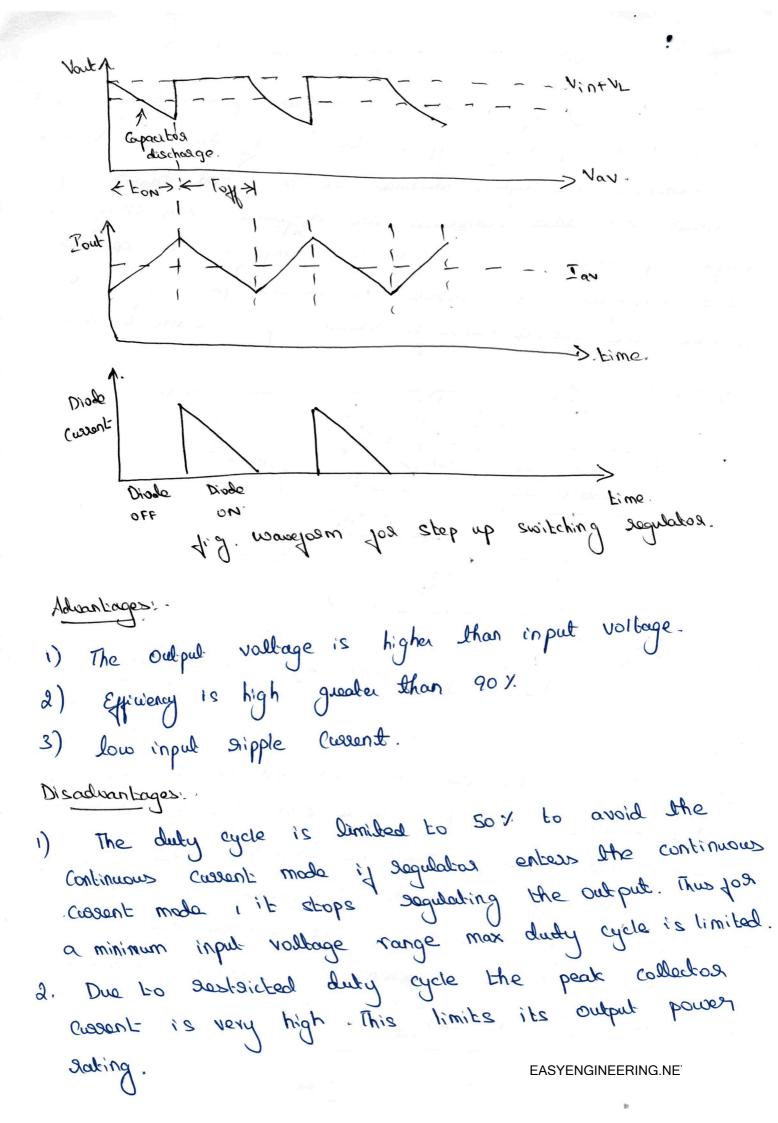
> EASTENGINEERING.NE

Expression Jos the output vollage.

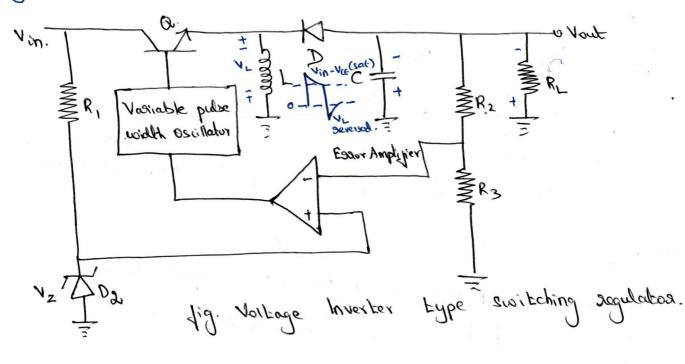
 $V_{out} = \frac{V_{in}}{8}$

VIN

Input



Voltage Investes type Switching Regulators (Buck-Boost) This type of Switching regulators (Buck-Boost) Voltage having polasity opposite to that of the input voltage. The elements are again identical to buck and boost type regulators but their connection are different. Any change in output produces esses which get amplified by op-amp esses amplifies. This Controls the ON LOFF period of Q to regulate the output through variable pulse width Oscillators.



wooking : -Case 1 :- The Q goes into saturation and the voltage across it daops to VCE (sal) which is about 0.3V. Due to this voltage acauss inductor suddonly riscs to [Vin-Vce (sat)] and. Magnetic field around it suddanly expands. Due to connection of diode D, in this situation it is several biased. The inductors voltage starts exponentially decreasing your the initial value [Vin - VCE (sat)].

Case 2! Now if B, is Evaned OFF, the magnetic field acaoss L get Collapsed but inductor cuesent can not change instantaneously. Thus voltage acases inductor NL sevence its polosity. Due to sovered NL, the dide D, is now forward biased. The capacitor charges through D, producing output Vollage of opposite poloaity to that of Vin Hence the regulation is called vallage inverter type. The sepecifive on off action of Q, produces a sepecifi changing and dischanging of the capacitors c which is smoothed by the LC filler action. The lass period Q is ON, higher is the output vollage, the greater time Q is on, Smaller is the Output voltage.

Pawer Supply performance and booking: The power Supply is the heart of any electronic equipment. Hence for the high quality and reliable operation it is necessary to verify the power supply performance by conducting the tests. The test specification much include all the safe operating limits such as temperature, line Condition, ragulation values else. The various stert equipment required to test a power supply age. (i) De power supply which is capable of supplying voltage and custoric for dynamic load which is capable of hondling various system requirements. EASYENGINEERING.NE

(iii) Accurate voltmeter, wattmeter and Ammeter iv) An oscillocrope with bandwidth 500 MHZ 02 MORE 0 vou measurement of noise. V) Network analyzer (a) prequency. response analyzer for Stability measurement. Testing Procedure and Specifications: The Various test used to check the peyosmance of a power Supply are discussed below. (i) Fiast switch on (j) Insush cussonli best-(iii) Transiest recovery time best (iv) static load segulation tests (V) line regulation test. (Vi) Periodic and Random desightion Lest (PARD) (Viii) Efficiency Lest (Viiii) Power Jackos. (ix) shoat up lime (X) Shool Cracuit output crosent (Xi) over voltage shut down (nii) lealage cueront (Killi) Hold up time.