JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

EC8351 – ELECTRONIC CIRCUITS 1

(Regulation 2017)

Year/Semester: II/03

2021 – 2022

Prepared by

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SYLLABUS

EC8351 **ELECTRONIC CIRCUITS 1** **L T P C 3 0 0 3**

OBJECTIVES:

- To understand the methods of biasing transistors
- To design and analyze single stage and multistage amplifier circuits
- To analyze the frequency response of small signal amplifiers
- To design and analyze the regulated DC power supplies.
- To troubleshoot and fault analysis of power supplies

UNIT I BIASING OF DISCRETE BJT, JFET AND MOSFET

BJT– Need for biasing — DC Load Line and Bias Point — DC analysis of Transistor circuits — Various biasing methods of BJT — Bias Circuit Design — Thermal stability — Stability factors — Bias compensation techniques using Diode, thermistor and sensistor — Biasing BJT Switching Circuits- JFET — DC Load Line and Bias Point — Various biasing methods of JFET — JFET Bias Circuit Design — MOSFET Biasing — Biasing FET Switching Circuits.

UNIT II BJT AMPLIFIERS

Small Signal Hybrid p equivalent circuit of BJT — Early effect — Analysis of CE, CC and CB amplifiers using Hybrid p equivalent circuits — AC Load Line Analysis- Darlington Amplifier — Bootstrap technique — Cascade, Cascode configurations — Differential amplifier, Basic BJT differential pair — Small signal analysis and CMRR.

UNIT III SINGLE STAGE FET, MOSFET AMPLIFIERS

Small Signal Hybrid p equivalent circuit of FET and MOSFET — Analysis of CS, CD and CG amplifiers using Hybrid p equivalent circuits — Basic FET differential pair- BiCMOS circuits.

UNIT IV FREQUENCY RESPONSE OF AMPLIFIERS

Amplifier frequency response — Frequency response of transistor amplifiers with circuit capacitors — BJT frequency response — short circuit current gain — cut off frequency — fa, fß and unity gain bandwidth — Miller effect — frequency response of FET — High frequency analysis of CE and MOSFET CS amplifier — Transistor Switching Times.

UNIT V POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

Linear mode power supply — Rectifiers — Filters — Half-Wave Rectifier Power Supply — Full- Wave Rectifier Power Supply — Voltage regulators: Voltage regulation — Linear series, shunt and switching Voltage Regulators — Over voltage protection — BJT and MOSFET — Switched mode power supply (SMPS) — Power Supply Performance and Testing — Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

TOTAL: 45 PERIODS

OUTCOMES:

After studying this course, the student should be able to:

- Acquire knowledge of ♣Working principles, characteristics and applications of BJT and FET♣Frequency response characteristics of BJT and FET amplifiers
- Analyze the performance of small signal BJT and FET amplifiers - single stage and multi stage amplifiers
- Apply the knowledge gained in the design of Electronic circuits

TEXT BOOKS:

1. Donald. A. Neamen, Electronic Circuits Analysis and Design, 3rd Edition, Mc Graw Hill Education (India) Private Ltd., 2010. (Unit I-IV)
2. Robert L. Boylestad and Louis Nasheresky, ―Electronic Devices and Circuit Theory‖, 11thEdition, Pearson Education, 2013. (Unit V)

REFERENCES

1. Millman J, Halkias.C.and Sathyabrada Jit, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2015.
2. Salivahanan and N. Suresh Kumar, Electronic Devices and Circuits, 4th Edition, , Mc Graw Hill Education (India) Private Ltd., 2017.
3. Floyd, Electronic Devices, Ninth Edition, Pearson Education, 2012.
4. David A. Bell, Electronic Devices & Circuits, 5th Edition, Oxford University Press, 2008.
5. Anwar A. Khan and Kanchan K. Dey, A First Course on Electronics, PHI, 2006.
6. Rashid M, Microelectronics Circuits, Thomson Learning, 2007

UNIT 3

3.1 JFET Amplifiers

It provides an excellent voltage gain with high input impedance. Due to these characteristics, it is often preferred over BJT.

Three basic FET configurations

Common source, common drain and common gate

3.2 JFET low frequency a.c Equivalent circuit

Figure shows the small signal low frequency a.c Equivalent circuit for n-channel JFET.

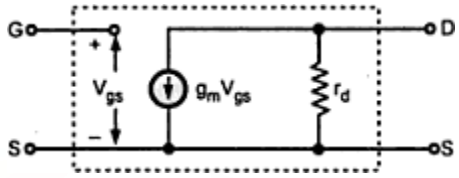


Fig3.1 small signal model of JFET

3.3 Common Source Amplifier With Fixed Bias

Figure shows Common Source Amplifier With Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis.

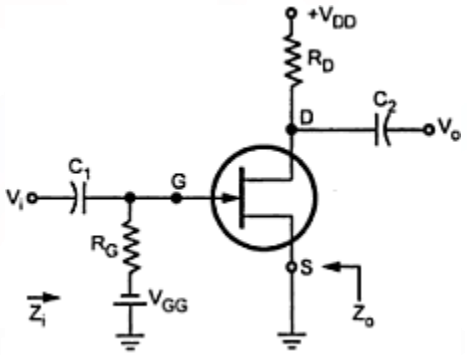


Fig3.2 Common source circuit of JFET

The following figure shows the low frequency equivalent model for Common Source Amplifier With Fixed Bias. It is drawn by replacing

- All capacitors and d.c supply voltages with short circuit
- JFET with its low frequency a.c Equivalent circuit

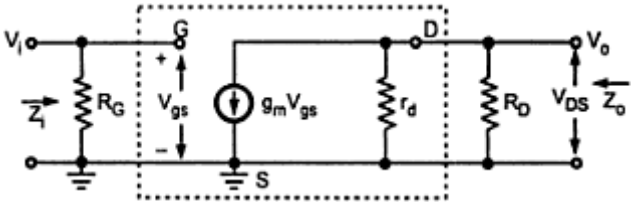


Fig3.3 small signal model of CS JFET amplifier

Input Impedance Zi

$Zi = R_G$

Output Impedance Zo

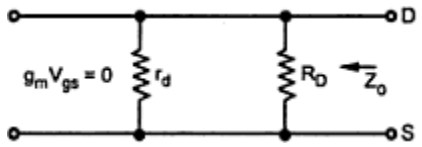


Fig3.4 Equivalent circuit model of JFET for output

It is the impedance measured looking from the output side with input voltage Vi equal to Zero. As Vi=0,Vgs =0 and hence g_mVgs =0 . And it allows current source to be replaced by an open circuit.

So,

$$Z_o = R_D \| r_d$$

If the resistance rd is sufficiently large compared to R_D, then

$$Z_o \approx R_D \qquad \because r_d >> R_D$$

Voltage Gain A_v :

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. we can write

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i (r_d \| R_D)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

and if $r_d >> R_D$,

$$A_v \approx -g_m R_D$$

Table summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d >> R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m (R_D \| r_d)$	$-g_m R_D$

3.4 Common source amplifier with self bias (Bypassed Rs)

Figure shows Common Source Amplifier With self Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

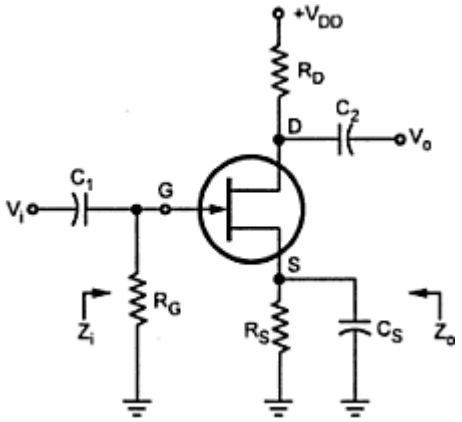


Fig3.5 **Common source amplifier** model of JFET

The following figure shows the low frequency equivalent model for Common Source Amplifier With self Bias.

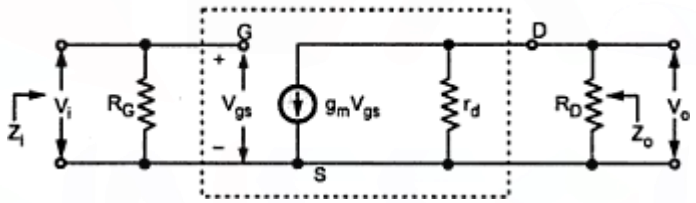


Fig3.6 **Small signal model for Common source amplifier** model of JFET

i) Input impedance Z_i : $Z_i = R_G$

ii) Output impedance Z_o : $Z_o = r_d \,||\, R_D$

if $r_d >> R_D$ $Z_o \approx R_D$

iii) Voltage gain A_v : $A_v = -g_m (r_d \,||\, R_D)$

If $r_d >> R_D$ $A_v = -g_m R_D$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

3.5 Common source amplifier with self bias (unbypassed Rs)

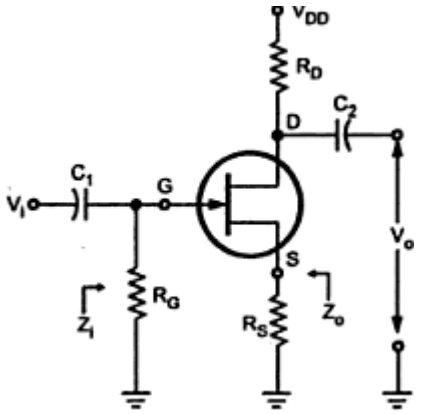


Fig3.7 **Common source amplifier** model of JFET

Now Rs will be the part of low frequency equivalent model as shown in figure.

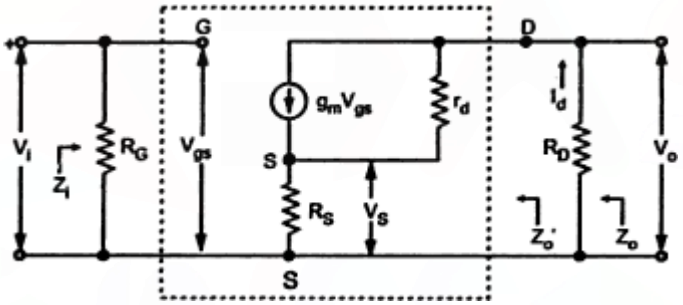


Fig3.8 **Small signal model for Common source amplifier** model of JFET

Input Impedance Zi

$Zi = R_G$

Output Impedance Zo

It is given by

$$Z_o = Z_o' \,||\, R_D$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

$$Z_o = [\, r_d + R_s\,(\mu + 1)\,] \,||\, R_D$$

$$Z_o = [\, r_d + R_s\,(g_m\, r_d + 1)\,] \,||\, R_D$$

Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

We know that,

$$V_o = -I_d R_D$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m r_d R_D}{r_d + R_s + R_D + g_m R_s r_d}$$

Dividing numerator and denominator by r_d we get,

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}}$$

If $r_d >> R_s + R_D$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s}$$

Table summarizes performance of common source amplifier with self bias.

Parameter	Bypassed R_S		Unbypassed R_S	
	Exact	$r_d >> R_D$	Exact	$r_d >> R_D$
Z_i	R_G	R_G	R_G	R_G
Z_o	$R_D \parallel r_d$	R_D	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$
A_v	$-g_m(R_D \parallel r_d)$	$-g_m R_D$	$\frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}}$	$\frac{-g_m R_D}{1 + g_m R_S}$

3.6 Common source amplifier with Voltage divider bias (Bypassed Rs)

Figure shows Common Source Amplifier With voltage divider Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

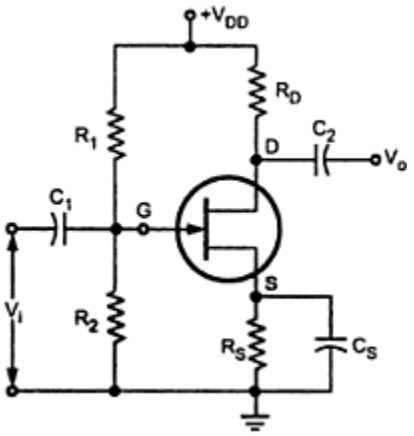


Fig3.9 **Common source amplifier with Voltage divider bias(Bypassed Rs)**

The following figure shows the low frequency equivalent model for Common Source Amplifier With voltage divider Bias

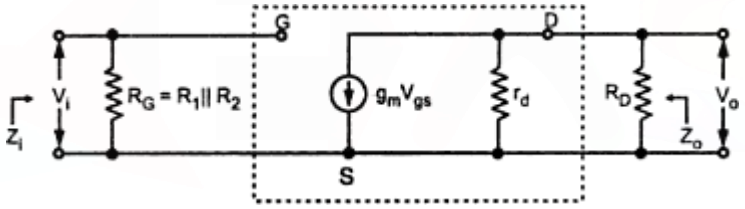


Fig3.10 **small model of Common source amplifier with Voltage divider bias(Bypassed Rs)**

The parameters are given by

$$R_G = R_1 \,||\, R_2$$

$$Z_i = R_G$$

$$= R_1 \,||\, R_2$$

$$Z_o = r_d \,||\, R_D$$

if $r_d >> R_D$

$$Z_o \approx R_D$$

$$A_v = -g_m (r_d \,||\, R_D)$$

If $r_d >> R_D$

$$A_v = -g_m R_D$$

The negative sign in the voltage gain indicates there is a 180^o phase shift between input and output voltages.

3.7 Common source amplifier with Voltage divider bias (unbypassed Rs)

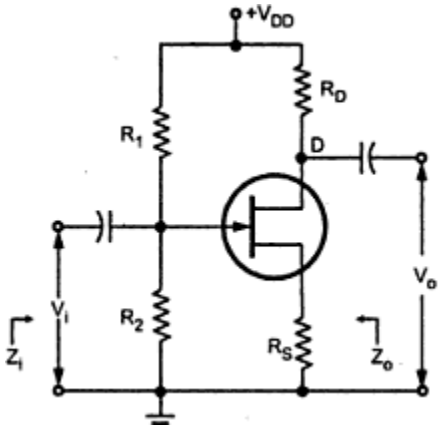
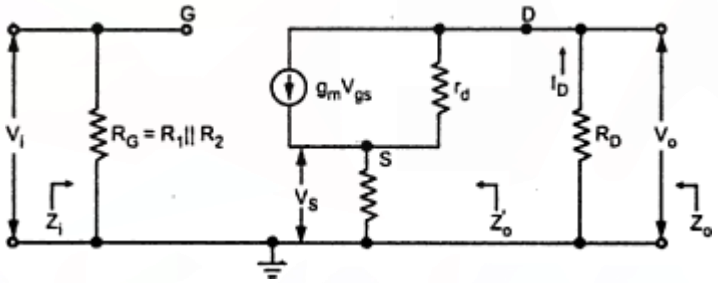


Fig3.11 **small model of Common source amplifier with Voltage divider bias(without Bypassed Rs)**

Now Rs will be the part of low frequency equivalent model as shown in figure.



It is important to note that, here, $R_G = R_1 \parallel R_2$.

$$Z_i = R_G = R_1 \parallel R_2$$

$$Z_o' = r_d + g_m R_s r_d + R_s$$

or

$$Z_o' = r_d + R_s (\mu + 1)$$

$$Z_o = [\, r_d + g_m R_s r_d + R_s \,] \parallel R_D$$

or

$$Z_o = [\, r_d + R_s (\mu + 1) \,] \parallel R_D$$

$$A_v = \frac{-g_m R_D}{1 + g_m R_s + \dfrac{R_s + R_D}{r_d}}$$

3.8 Common Drain Amplifier

In this circuit, input is applied between gate and source and output is taken between source and drain.

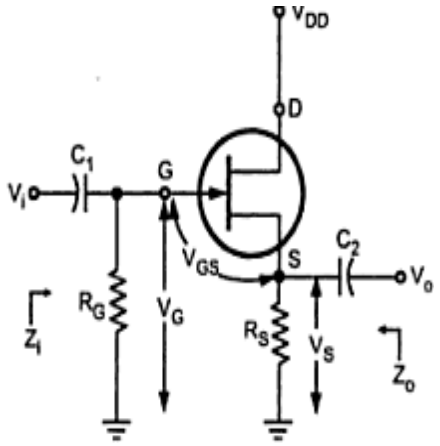


Fig3.12 **Circuit of Common Drain amplifier**

In this circuit, the source voltage is

$Vs = V_G + V_{GS}$

When a signal is applied to the JFET gate via C1 ,VG varies with the signal. As VGS is fairly constant and $Vs = V_G + V_{GS}$, Vs varies with Vi.

The following figure shows the low frequency equivalent model for common drain circuit.

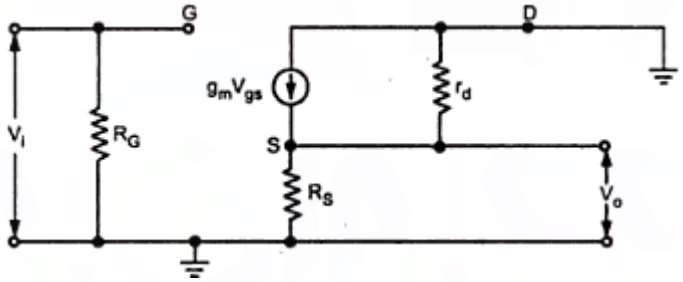


Fig3.13 **small model of Common Drain amplifier**

Input Impedance Zi

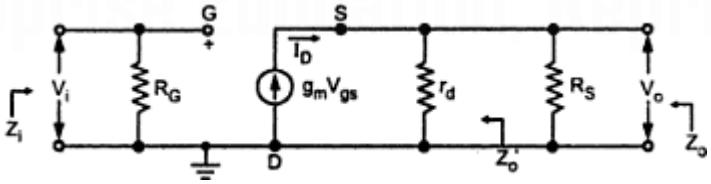


Fig3.13 Simplified small model of Common Drain amplifier

$Zi = R_G$

Output Impedance Zo

It is given by

$$Z_o = Z_o' || R_s$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0$$

As $$V_i = 0,$$

$$V_{gs} = V_o$$

Looking at Fig. we can write that,

$$g_m V_{gs} = I_d$$

But Vgs = Vo, so

$$g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

$$\therefore \quad Z_o = \frac{1}{g_m} || R_s$$

Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

Looking at Fig. we can write that,

$$V_o = - I_d (r_d || R_s)$$

and $$I_d = g_m V_{gs}$$

$$\therefore \quad V_o = - g_m V_{gs} (r_d || R_s)$$

But

$$V_i = - V_{gs} + V_o$$

$$= - V_{gs} + [- g_m V_{gs} (r_d || R_s)]$$

Substitute the value Vo and Vi. Then

$$A_v = \frac{-g_m V_{gs} (r_d \,||\, R_s)}{-V_{gs} (1 + g_m (r_d \,||\, R_s))}$$

$$= \frac{g_m (r_d \,||\, R_s)}{1 + g_m (r_d \,||\, R_s)}$$

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

if $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one.

Common drain circuit does not provide voltage gain.& there is no phase shift between input and output voltages.

Table summarizes the performance of common drain amplifier

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \,\|\|\, R_s$	$\frac{1}{g_m} \,\|\|\, R_s$
A_v	$\frac{g_m (r_d \,\|\|\, R_s)}{1 + g_m (r_d \,\|\|\, R_s)}$	$\frac{g_m R_s}{1 + g_m R_s}$

3.9 Common Gate Amplifier

In this circuit, input is applied between source and gate and output is taken between drain and gate.

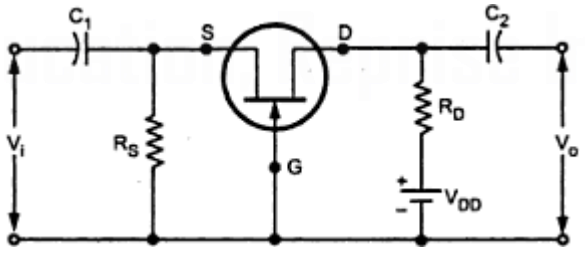


Fig3.14 **Circuit diagram of Common gate amplifier**

In CG Configuration, gate potential is at constant potential. so, increase in input voltage Vi in positive direction increase the negative gate source voltage. Due to I_D reduces, reduces, reducing the drop I_DR_D. Since $V_D = V_{DD} - I_DR_D$, the reduction in I_D results in an increase in output voltage.

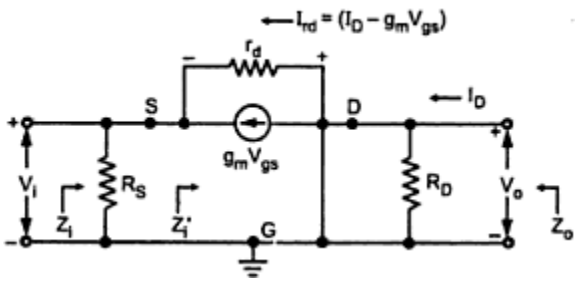


Fig3.15 **small signal model for Common gate amplifier**

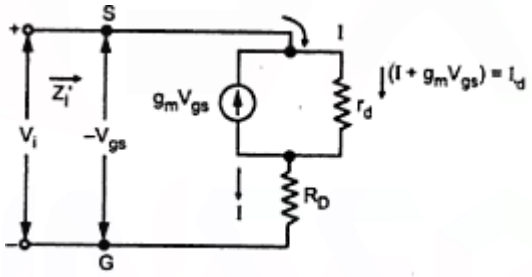
1. Input Impedance (Zi)

It is given by

$$Z_i = R_s \parallel Z_i'$$

And

$$Z_i' = \frac{V_i}{I}$$



$$I_{rd} = I + g_m V_{gs}$$

$$\therefore \quad I = I_{rd}\ g_m V_{gs}$$

where $$I_{rd} = \frac{V_i - IR_D}{r_d}$$

After substituting and simplification,

$$\frac{V_i}{I} = \frac{1 + \frac{R_D}{r_d}}{\frac{1}{r_d} + g_m} = \frac{r_d + R_D}{1 + g_m r_d}$$

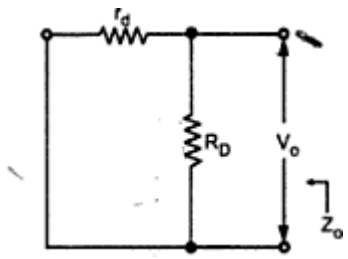
And

$$Z_i = R_s \parallel Z_i' = R_s \parallel \frac{r_d + R_D}{1 + g_m r_d}$$

If $r_d >> R_D$ and $g_m r_d >> 1$ then we can write,

$$Z_i = R_s \| \frac{r_d}{g_m r_d} = R_s \| \frac{1}{g_m}$$

2. Output Impedance Zo



It is given by

$$Z_o = r_d \| R_D$$

If $r_d >> R_D$

$$Z_o \approx R_D$$

3. Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -I_D R_D$$

$$V_i = -V_{gs}$$

Using KVL to the outer loop, after simplification

$$A_v = \frac{V_o}{V_i} = \frac{-I_d + R_D}{\frac{-I_d(r_d + R_D)}{1 + g_m r_d}}$$

$$= \frac{R_D(1 + g_m r_d)}{r_d + R_D}$$

If $r_d >> R_D$ and $g_m r_d >> 1$

$$A_v = \frac{R_D(g_m r_d)}{r_d} = R_D g_m$$

Table summarizes the performance of common gate amplifier

	Exact	$r_d >> R_{DD}$
Z_i	$R_s \parallel \left[\frac{r_d + R_D}{1+g_m r_d}\right]$	$R_s \parallel \frac{1}{g_m}$
Z_o	$r_d \parallel R_D$	R_D
A_v	$\frac{R_D(1+g_m r_d)}{r_d + R_D}$	$g_m R_D$

3.10 Multistage Amplifiers

In practice, we need amplifier which can amplify a signal from a very weak source such as a microphone, to a level which is suitable for the operation of another transducer
such as loudspeaker . This is achieved by cascading number of amplifier stages, known as multistage amplifier

1. Need for Cascading

For faithful amplification amplifier should have desired voltage gain, current gain and it should match its input impedance with the source and output impedance with the load. Many times these primary requirements of the amplifier can not be achieved with single stage amplifier, because of the limitation of the transistor/FET parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.
We can say that,

- When the amplification of a single stage amplifier is not sufficient, or,
- When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier, with two or more stages is also known as multistage amplifier.

2. Two Stage Cascaded Amplifier

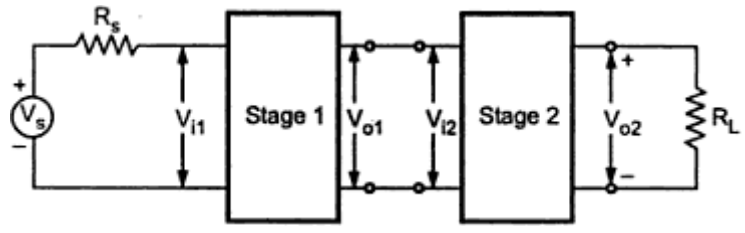


Fig3.16 **Cascaded amplifier**

Vi1 is the input of the first stage and Vo2 is the output of second stage.
So,Vo2/Vi1 is the overall voltage gain of two stage amplifier.

$$A_V = \frac{V_{o2}}{V_{i1}}$$

$$= \frac{V_{o2}}{V_{i2}} \frac{V_{i2}}{V_{i1}}$$

$$V_{o1} = V_{i2}$$

$$\therefore A_V = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}}$$

$$= A_{V2} A_{V1}$$

3. n-Stage Cascaded Amplifier

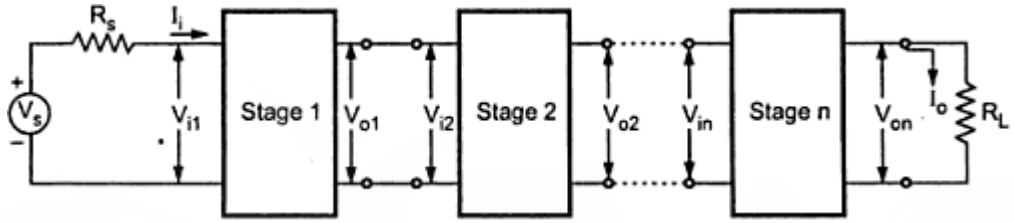


Fig3.17 Multistage **amplifier**

Voltage gain :

The resultant voltage gain of the multistage amplifier is the product of voltage gains of the various stages.

Av = Avl Av2 ... Avn

Gain in Decibels

In many situations it is found very convenient to compare two powers on logarithmic scale rather than on a linear scale. The unit of this logarithmic scale is called decibel (abbreviated dB). The number N decibels by which a power P2 exceeds the power P1 is defined by

$$N = 10 \log \frac{P_2}{P_1}$$

Decibel, dB denotes power ratio. Negative values of number of dB means that the power P2 is less than the reference power P1 and positive value of number of dB means the power P2 is greater than the reference power P1.

For an amplifier, P1 may represent input power, and P2 may represent output power. Both can be given as

$$P_1 = \frac{V_i^2}{R_i} \text{ and } P_2 = \frac{V_o^2}{R_o}$$

Where Ri and Ro are the input and output impedances of the amplifier respectively.Then,

$$N = 10 \log_{10} \frac{V_o^2 / R_o}{V_i^2 / R_i}$$

If the input and output impedances of the amplifier are equal i.e. Ri = Ro= R, then

$$N = 10 \log_{10} \frac{V_o^2}{V_i^2} = 10 \log_{10} \left(\frac{V_o^2}{V_i^2} \right) = 10 \times 2 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{V_o}{V_i}$$

4. Gain of Multistage Amplifier in dB

The gain of a multistage amplifier can be easily calculated if the gain of the individual stages are known in dB, as shown below

$20 \log_{10} Av = 20 \log_{10} Avl + 20 \log_{10} Av2 + \ldots + 20 \log_{10} Avn$

Thus, the overall voltage gain in dB of a multistage amplifier is the decibel voltage gains of the individual stages. It can be given as

$AvdB = AvldB + Av2dB + ... + AvndB$

Advantages of Representation of Gain in Decibels

Logarithmic scale is preferred over linear scale to represent voltage and power gains because of the following reasons :

- In multistage amplifiers, it permits to add individual gains of the stages to calculate overall gain.
- It allows us to denote, both very small as well as very large quantities of linear, scale by considerably small figures.

  For example, voltage gain of 0.0000001 can be represented as -140 dB and voltage gain of 1,00,000 can be represented as 100 dB.
- Many times output of the amplifier is fed to loudspeakers to produce sound which is received by the human ear. It is important to note that the ear responds to the sound intensities on a proportional or logarithmic scale rather than linear scale. Thus use of dB unit is more appropriate for representation of amplifier gains.

3.11 Small signal Analysis of MOSFET

Common-Source Configuration

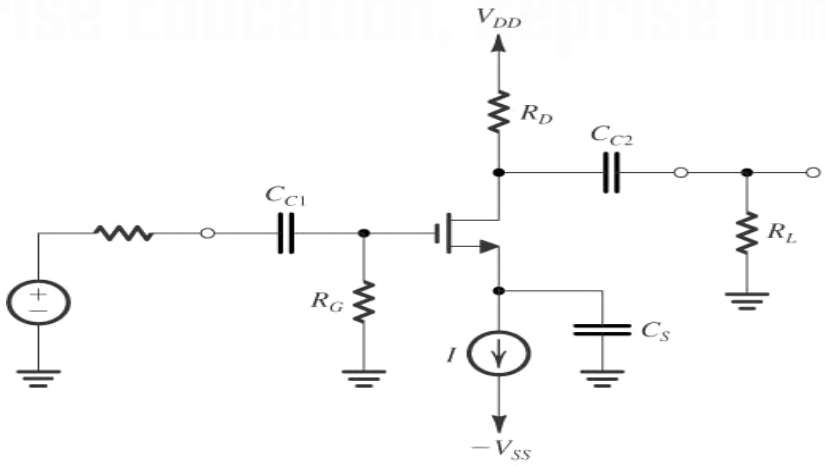


Fig3.17 ***Common-Source Configuration of MOSFET***

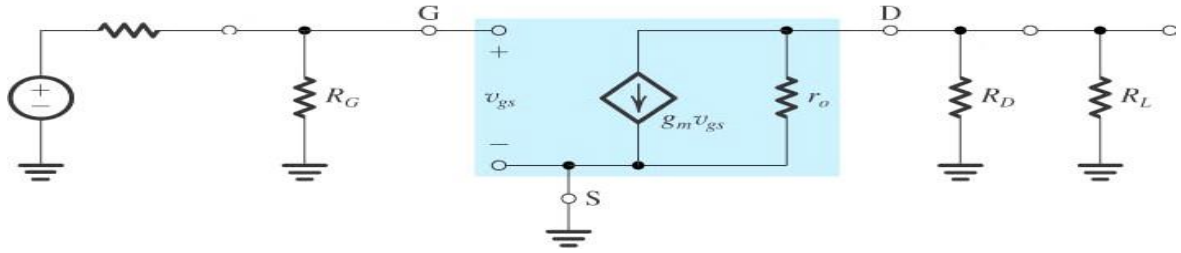


Fig3.18 small signal model of ***Common-Source Configuration of MOSFET***

$$R_{in} = R_G$$

$$R_o = r_o \,//\, R_D$$

$$A_{vo} = -g_m \cdot (r_o \,//\, R_D)$$

This configuration serves as the gain stage. The disadvantage is high output impedance. Capacitor *CS* is included such that the stage is connected to a current source for biasing

Common-Gate Configuration

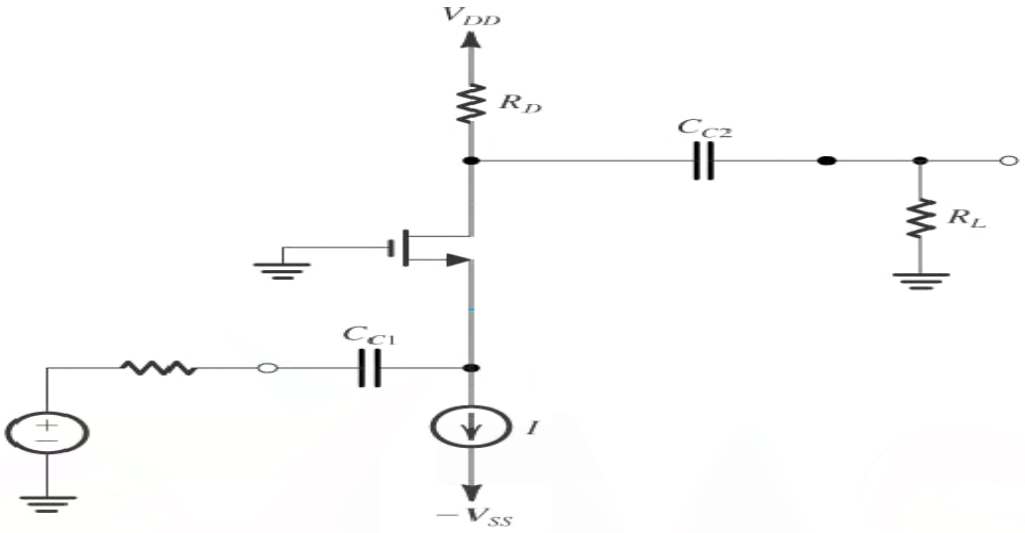


Fig3.18 ***Common-gate Configuration of MOSFET***

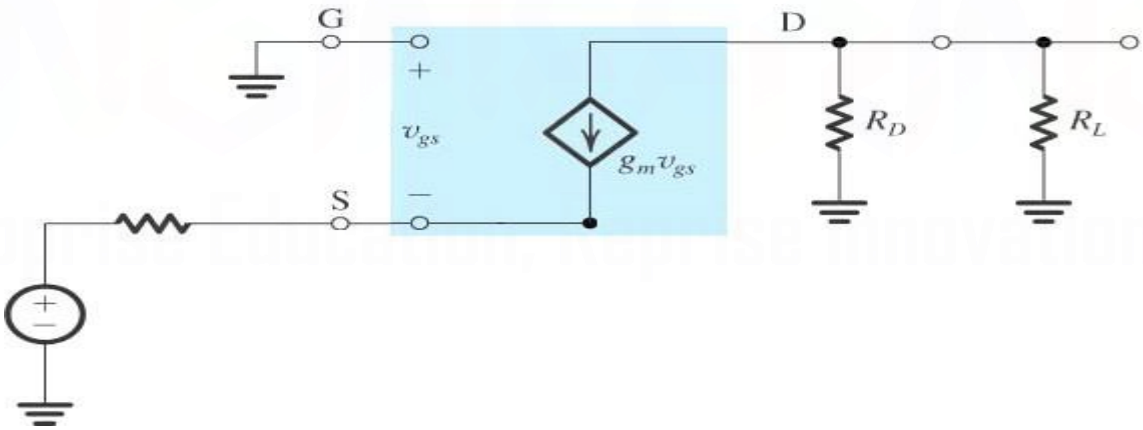


Fig3.18 small signal model of ***Common-gate Configuration of MOSFET***

$$R_{in} = \frac{1}{g_m}$$

$$R_o = R_D$$

$$A_{vo} - g_m \cdot R_D$$

This amplifier provides gain and is useful when a specific (low) *Rin* is required. This is, e.g., the case when the impedance needs to be matched, as with transmission lines (e.g. to 50 Ω). Another application of the CG configuration is that it acts as a current buffer (current gain close to unity, small *Rin*, large *Rout*).

Source Follower (Common-Drain Configuration)

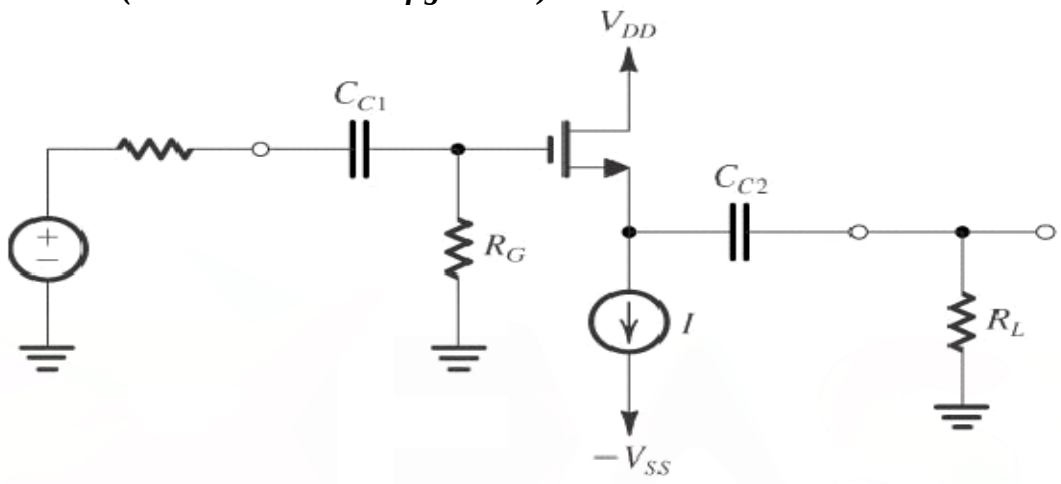


Fig3.19 ***Common-drain Configuration of MOSFET***

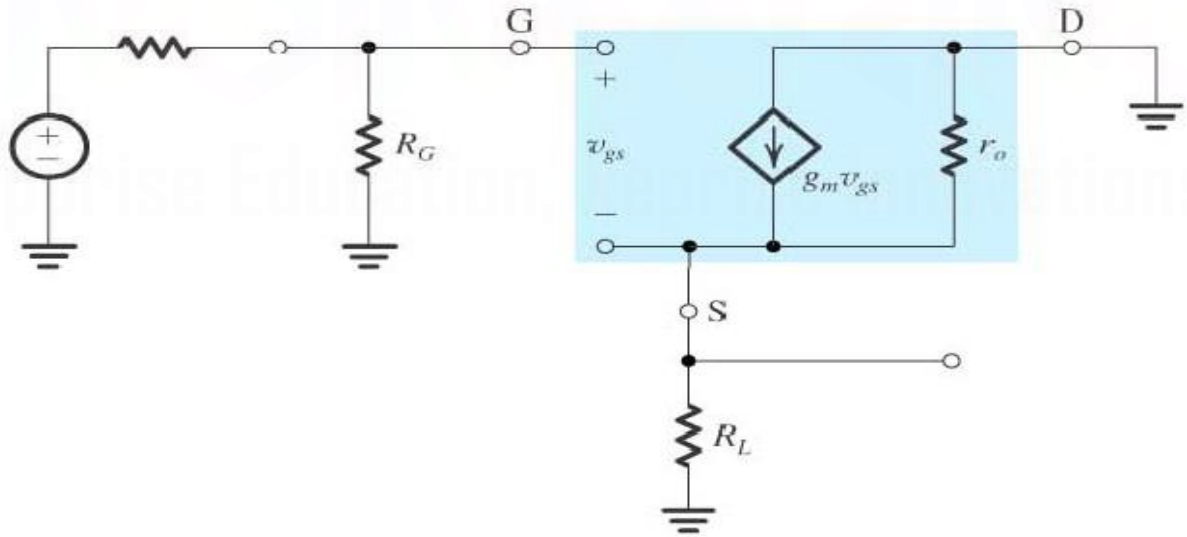


Fig3.20 small signal model of ***Common-drain Configuration of MOSFET***

$$R_{in} = R_G$$

$$R_o = r_o // \frac{1}{g_m} \approx \frac{1}{g_m}$$

$$A_{vo} = \frac{g_m \cdot r_o}{1 + g_m \cdot r_o}$$

This configuration acts as a voltage buffer. It provides no gain, but has low output impedance. It is typically the last stage in a multi-stage amplifier.

3.12 Cascaded Amplifiers

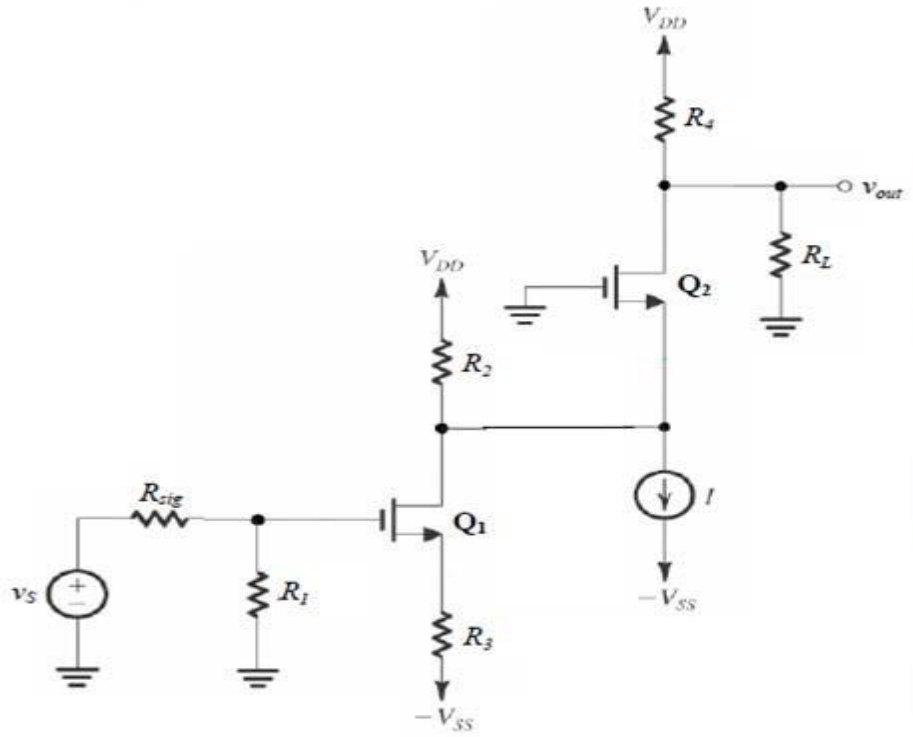


Fig3.21 Cascaded amplifier ***Configuration of MOSFET***

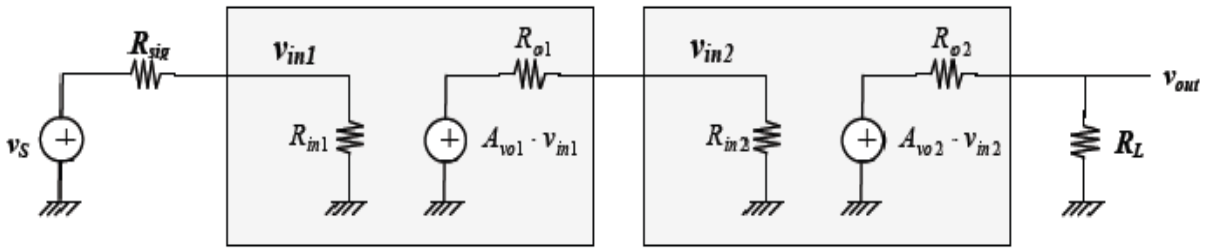


Fig3.20 small signal model of Cascaded ***Configuration of MOSFET***

$$A_{vo1} = -\frac{g_{m1} \cdot R_2}{1 + g_{m1} \cdot R_3}$$
$$A_{vo2} = g_{m2} \cdot R_4$$
$$R_{o1} = R_2$$
$$R_{o2} = R_4$$
$$R_{in1} = R_1$$
$$R_{in2} = \frac{1}{g_{m2}}$$

By grouping the different factors in this expression, we can find a physical interpretation for the cascading. This physical interpretation can be used to guide simulation or analysis of the different stages separately, before combining them into a cascaded amplifier.

$$\frac{v_{out}}{v_S} = \frac{v_1}{v_S} \cdot \frac{v_{out}}{v_2} = \underbrace{\left[\frac{R_{in1}}{R_{in1} + R_S} \cdot A_{vo1} \cdot \frac{R_{in2}}{R_{in2} + R_{o1}}\right]}_{\text{Gain of stage 1 with actual source and loaded by stage 2}} \cdot \underbrace{\left[A_{vo2} \cdot \frac{R_L}{R_L + R_{o2}}\right]}_{\text{Gain of stage 2 with ideal source and loaded by } R_L}$$

QUESTIONS

2 MARKS

1. What is meant by small signal?
2. What is the physical meaning of small signal parameter ro?
3. Write the equation for small signal condition that must be satisfied for linear amplifiers.
4. Draw the small signal equivalent circuit common source NMOS.
5. What is another name for common drain amplifier?
6. Draw the source follower amplifier circuit.
7. List the applications of MOSFET amplifiers.
8. Compare the characteristics of three MOSFET amplifier configurations.
9. Draw the small signal equivalent JFET common source circuit.
10. How does a transistor width-to-length ratio affect the small signal voltage gain of a common source amplifier?
11. How a MOSFET can be used to amplify a time varying voltage?
12. How does body effect change the small signal equivalent of the MOSFET?
13. Why in general the magnitude of the voltage gain of a common source amplifier relatively small?
14. What is voltage swing limitation?
15. What is the general condition under which a common gate amplifier would be used?

16. State the general advantage of using transistors in place of resistors in integrated circuits.
17. Give one reason why a JFET might be used as an input device in a circuit as proposed to a MOSFET.
18. What are features of cascode amplifiers?
19. What are the applications of BiCMOS?
20. Discuss one advantage of BiCMOS circuit.

16 MARKS

1. Describe the operation and analyze the basic JFET amplifier circuits.
2. Derive the small signal analysis of common source amplifier.
3. Develop a small signal model of JFET device and analyze basic JFET amplifiers.
4. Explain graphically the amplification process in a simple MOSFET amplifier circuit.
5. Describe the small signal equivalent circuit of the MOSFET and determine the values of small signal parameters?
6. Sketch the small signal high frequency circuit of a common source amplifier & derive the expression for a voltage gain, input & output admittance and input capacitance.
7. Sketch a simple source-follower amplifier circuit and discuss the general ac circuit characteristics.
8. Characterize the voltage gain and output resistance of a common-gate amplifier.
9. Apply the MOSFET small signal equivalent circuit in the analysis of multistage amplifier circuits.
10. Explain common source amplifier with source resistor and source bypass capacitor.
11. Write short notes Voltage swing limitations, general conditions under which a source follower amplifier would be used.
12. Describe the characteristics of and analyze BiCMOS circuits.