JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

EC8351 – ELECTRONIC CIRCUITS 1

(Regulation 2017)

Year/Semester: II/03

2021 – 2022

Prepared by

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SYLLABUS

EC8351 **ELECTRONIC CIRCUITS 1** **L T P C 3 0 0 3**

OBJECTIVES:

- To understand the methods of biasing transistors
- To design and analyze single stage and multistage amplifier circuits
- To analyze the frequency response of small signal amplifiers
- To design and analyze the regulated DC power supplies.
- To troubleshoot and fault analysis of power supplies

UNIT I BIASING OF DISCRETE BJT, JFET AND MOSFET

BJT– Need for biasing — DC Load Line and Bias Point — DC analysis of Transistor circuits — Various biasing methods of BJT — Bias Circuit Design — Thermal stability — Stability factors — Bias compensation techniques using Diode, thermistor and sensistor — Biasing BJT Switching Circuits- JFET — DC Load Line and Bias Point — Various biasing methods of JFET — JFET Bias Circuit Design — MOSFET Biasing — Biasing FET Switching Circuits.

UNIT II BJT AMPLIFIERS

Small Signal Hybrid p equivalent circuit of BJT — Early effect — Analysis of CE, CC and CB amplifiers using Hybrid p equivalent circuits — AC Load Line Analysis- Darlington Amplifier — Bootstrap technique — Cascade, Cascode configurations — Differential amplifier, Basic BJT differential pair — Small signal analysis and CMRR.

UNIT III SINGLE STAGE FET, MOSFET AMPLIFIERS

Small Signal Hybrid p equivalent circuit of FET and MOSFET — Analysis of CS, CD and CG amplifiers using Hybrid p equivalent circuits — Basic FET differential pair- BiCMOS circuits.

UNIT IV FREQUENCY RESPONSE OF AMPLIFIERS

Amplifier frequency response — Frequency response of transistor amplifiers with circuit capacitors — BJT frequency response — short circuit current gain — cut off frequency — fa, fß and unity gain bandwidth — Miller effect — frequency response of FET — High frequency analysis of CE and MOSFET CS amplifier — Transistor Switching Times.

UNIT V POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

Linear mode power supply — Rectifiers — Filters — Half-Wave Rectifier Power Supply — Full- Wave Rectifier Power Supply — Voltage regulators: Voltage regulation — Linear series, shunt and switching Voltage Regulators — Over voltage protection — BJT and MOSFET — Switched mode power supply (SMPS) — Power Supply Performance and Testing — Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

TOTAL: 45 PERIODS

OUTCOMES:

After studying this course, the student should be able to:

- Acquire knowledge of ♣Working principles, characteristics and applications of BJT and FET♣Frequency response characteristics of BJT and FET amplifiers
- Analyze the performance of small signal BJT and FET amplifiers - single stage and multi stage amplifiers
- Apply the knowledge gained in the design of Electronic circuits

TEXT BOOKS:

1. Donald. A. Neamen, Electronic Circuits Analysis and Design, 3rd Edition, Mc Graw Hill Education (India) Private Ltd., 2010. (Unit I-IV)
2. Robert L. Boylestad and Louis Nasheresky, ―Electronic Devices and Circuit Theory‖, 11thEdition, Pearson Education, 2013. (Unit V)

REFERENCES

1. Millman J, Halkias.C.and Sathyabrada Jit, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2015.
2. Salivahanan and N. Suresh Kumar, Electronic Devices and Circuits, 4th Edition, , Mc Graw Hill Education (India) Private Ltd., 2017.
3. Floyd, Electronic Devices, Ninth Edition, Pearson Education, 2012.
4. David A. Bell, Electronic Devices & Circuits, 5th Edition, Oxford University Press, 2008.
5. Anwar A. Khan and Kanchan K. Dey, A First Course on Electronics, PHI, 2006.
6. Rashid M, Microelectronics Circuits, Thomson Learning, 2007

UNIT II BJT AMPLIFIERS

2.1 Introduction

An amplifier is used to increase the signal level. It is used to get a larger signal output from a small signal input. Assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform with frequency same as that of input. To make the transistor work as an amplifier, it is to be biased to operate in active region. It means base-emitter junction is forward biased and base-collector junction is reverse biased.

Let us consider the common emitter amplifier circuit using voltage divider bias.

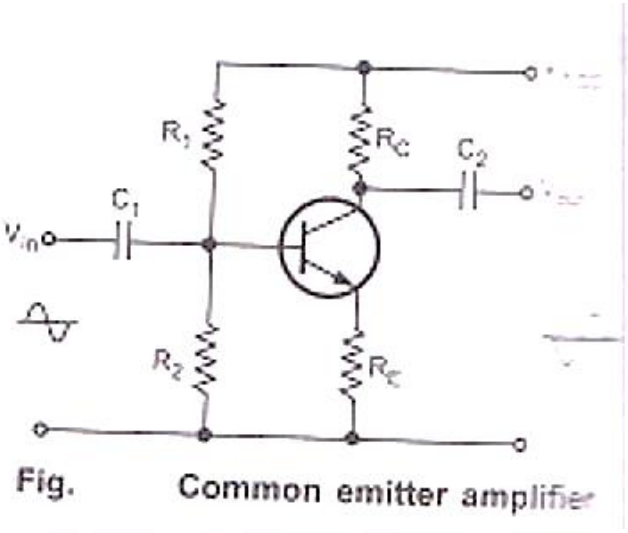
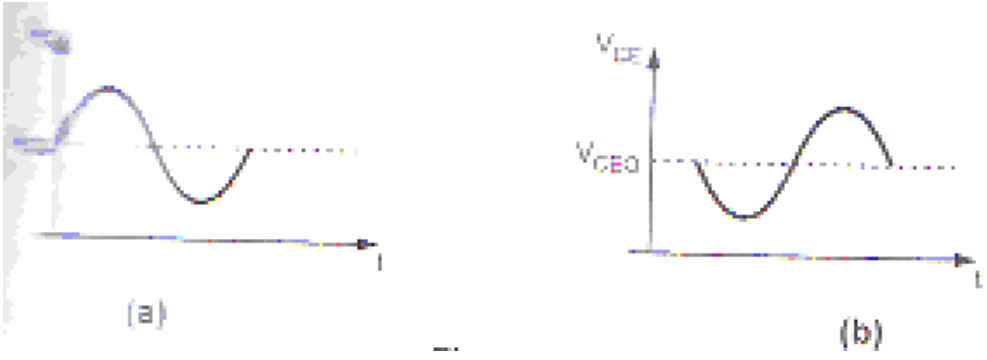


Fig. Common emitter amplifier

In the absence of input signal, only D.C. voltage is present in the circuit. It is known as zero signal or no signal condition or quiescent condition. D.C. collector-emitter voltage V_{CE}, D.C. collector current I_C and base current I_B is the quiescent operating point for the amplifier. Due to this base current varies sinusoidaly as shown in the below figure. Fig. I_{BQ} is quiescent DC base current

If the transistor is biased to operate in active region, output is linearly proportional to the input. The collector current is β times larger than the input base current in CE configuration. The collector current will also vary sinusoidally about its quiescent value I_{CQ}. The output voltage will also vary sinusoidally as shown in the below figure.



Variations in the collector current and voltage between collector and emitter due to change in base current are shown graphically with the help of load line in the above figure.

2.2 Common Emitter Amplifier Circuit

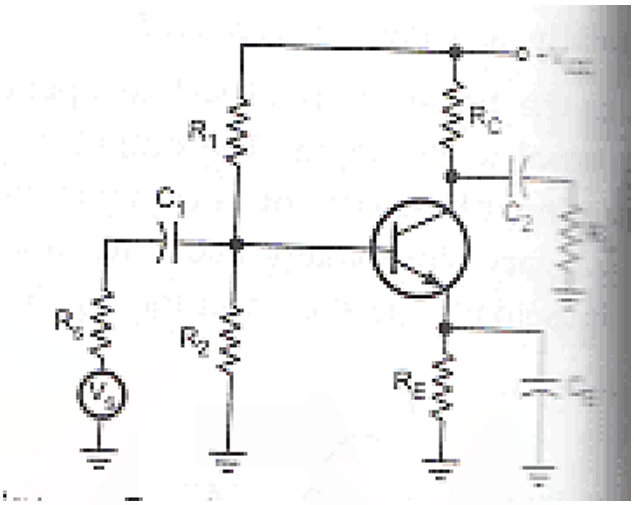


Fig. Practical common-emitter amplifier circuit

From above circuit, it consists of different circuit components. The functions of these components are as follows:

1. **Biasing Circuit:**

Resistors R_1, R_2 and R_E forms the voltage divider biasing circuit for CE amplifier and it sets the proper operating point for CE amplifier.

2. **Input Capacitor C_1:**

C_1 couples the signal to base of the transistor. It blocks any D.C. component present in the signal and passes only A.C. signal for amplification.

3. **Emitter Bypass Capacitor C_E:**

C_E is connected in parallel with emitter resistance R_E to provide a low reactance path to the amplified A.C. This will reduce the output voltage and reducing the gain value.

4. **Output Coupling Capacitor C_2:**

C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks D.C. and passes only A.C. part of the amplified signal.

Need for C_1, C_2, and C_E:

The impedance of the capacitor is given by,

$X_C = 1/ (2\prod f_c)$

Phase reversal:

The phase relationship between the input and output voltages can be determined by considering the effect of positive and negative half cycle separately. The collector current is β times the base current, so the collector current will also increases. This increases the voltage drop across R_C.

$V_C = V_{CC} - I_C R_C$

Increase in I_C results in a drop in collector voltage $V_{C,}$ as V_{CC} is constant. V_i increases in a positive direction, V_o goes in negative direction and negative half cycle of output voltage can be obtained for positive half cycle at the input.

In negative half cycle of input, A.C. and D.C. voltage will oppose each other. This will reduce the base current. Accordingly collector current and drop across R_C both will reduce and it increases the output voltage. So positive half cycle at the output for negative half cycle at the input can be obtained. So there is a phase shift of 180º between input and output voltages for a common emitter amplifier.

2.3 Common Collector Amplifier Circuit:

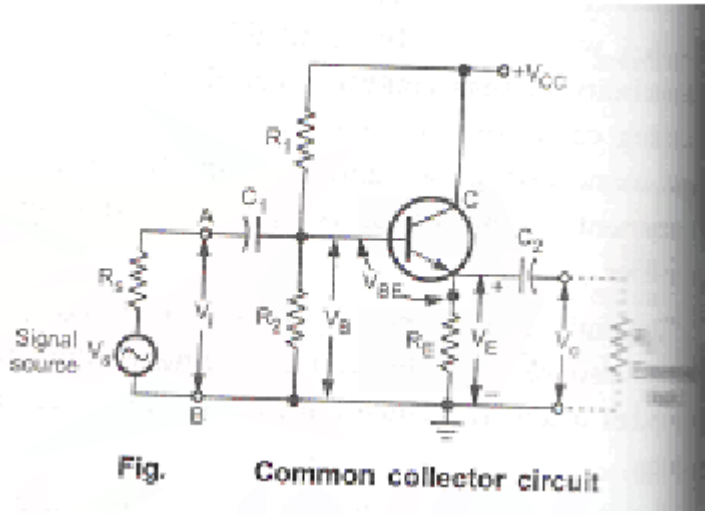


Fig. Common collector circuit

From above circuit, D.C. biasing is provided by R_1, R_2 and R_E. The load resistance is capacitor coupled to the emitter terminal of the transistor. When a signal is applied to base of the transistor, V_B is increased and decreased as the signal goes positive and negative respectively.

From figure, VE = VB - V_{BE}

Consider V_{BE} is constant, so the variation in V_B appears at emitter and emitter voltage V_E will vary same as base voltage V_B. In common collector circuit, emitter terminal follows the signal voltage applied to the base. It is also known as emitter follower.

2.4 Common Base Amplifier Circuit:

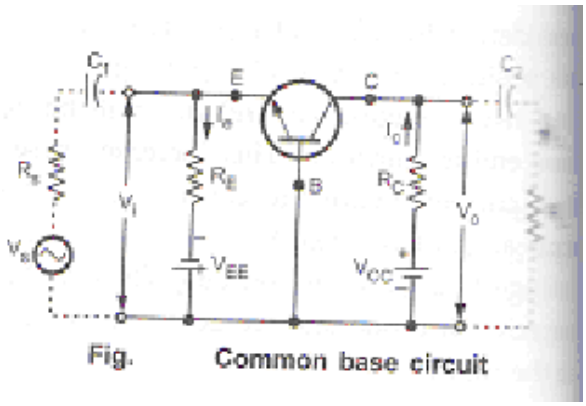


Fig. Common base circuit

From above circuit, the signal source is coupled to the emitter of the transistor through C_1. The load resistance R_L is coupled to the collector of the transistor through C_2. The positive going pulse of input source increases the emitter voltage. As base voltage is constant, forward bias of emitter-base junction reduces. This reduces I_b, I_c and drop across R_c.

$$V_o = V_{CC} - I_C R_C$$

Reduction in I_C results in an increase in V_o. Positive going input produces positive going output and vice versa. So there is no phase shift between input and output in common base amplifier.

2.5 Small Signal Low Frequency h-parameter Model:

Let us consider the transistor amplifier as a block box.

Fig. Transistor amplifier

Where, I_i – input current to the amplifier
V_i - input voltage to the amplifier
I_o – output current of the amplifier
V_o – output voltage of the amplifier

Input current is an independent variable. Input voltage and output current are dependent variables. Input current and output voltage are independent variables.

$$V_i = f_1(I_i, V_o)$$
$$I_o = f_2(I_i, V_o)$$

This can be written in the equation form as,

$$V_i = h_{11} I_i + h_{12} V_o$$
$$I_o = h_{21} I_i + h_{22} V_o$$

The above equation can also be written using alphabetic notations,

$$V_i = h_i \cdot I_i + h_r \cdot V_o$$
$$I_o = h_f \cdot I_i + h_o \cdot V_o$$

Definitions of h-parameter:

The parameters in the above equations are defined as follows:

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$$

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}$$

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$$

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}$$

h_{11} – input resistance with output short-circuited in ohms
h_{12} – fraction of output voltage at input with input open circuited, it is unitless
h_{21} – forward current transfer ratio or current gain with output short circuited, it is unitless
h_{22} – output admittance with input open circuited in mhos

Benefits of h-parameters:

1. Real numbers at audio frequencies
2. Easy to measure
3. Can be obtained from the transistor static characteristic curve
4. Convenient to use in circuit analysis and design
5. Most of the transistor manufacturers specify the h-parameters

2.6 h-Parameters for all three configurations:

Transistor can be represented as two port network by making anyone terminal common between input and output. There are three possible configurations in which a transistor can be used, there is a change in terminal voltage and current for different transistor configurations. To designate the type of configuration another subscript is added to h-parameters.

$h_{ie} = h_{11e}$– input resistance in CE configuration
$h_{fb} = h_{21b}$ – short circuit current gain in CB configuration

Table: Summarizes h-parameters for all three configurations

Parameter	CB	CE	CC
Input resistance	h_{ib}	h_{ie}	h_{ic}
Reverse voltage gain	h_{rb}	h_{re}	h_{rc}
Forward transfer current gain	h_{fb}	h_{fe}	h_{fc}
Output admittance	h_{ob}	h_{oe}	h_{oc}

The basic circuit of hybrid model is same for all three configurations, only parameters are different.

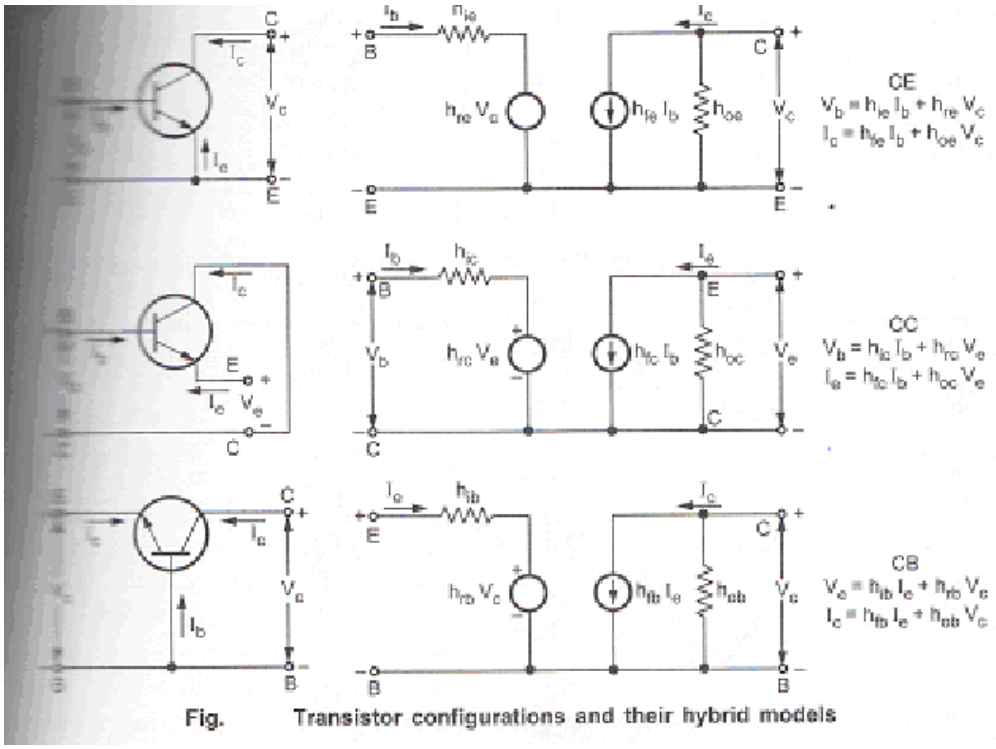


Fig. Transistor configurations and their hybrid models

The circuit and equations are valid for either NPN or PNP transistor and are independent of the type of load or method of biasing.

Determination of h-parameters from characteristics:

Consider CE configuration, its functional relationship can be defined from the following equations:

$$V_{be} = f_1 (I_b , V_{ce})$$
$$I_c = f_2 (I_b , V_{ce})$$

The input characteristic curve gives the relationship between input voltage V_{BE} and input current I_B for different values of output voltage V_{CE}. The following figure shows the typical input characteristic curve for CE configuration.

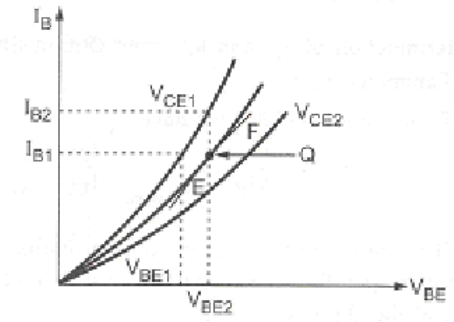


Fig. Typical input characteristic curves for the common emitter transistor configuration

Determination of h_{ie} and h_{re} from characteristic curve:

Parameter h_{ie}:

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\text{ constant}} = \frac{V_{BE2} - V_{BE1}}{I_{B2} - I_{B1}}$$

Parameter h_{re}:

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B\text{constant}} = \frac{V_{BE2} - V_{BE1}}{V_{CE2} - V_{CE1}}$$

The output characteristic curve gives the relationship between output current I_C and output voltage V_{CE} for different values of input current I_B.

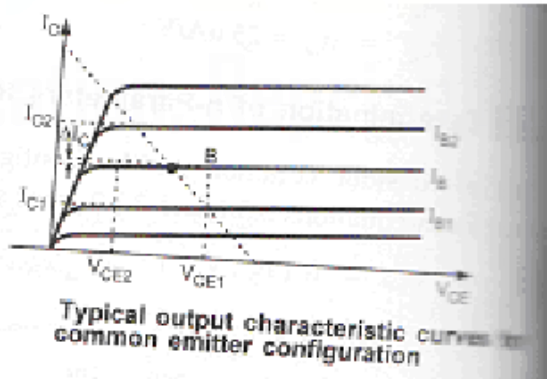


Fig. Typical output characteristic curves for common emitter configuration

Determination of h_{fe} and h_{oe} from output characteristic curve:

Parameter h_{fe}:

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\text{constant}} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

Parameter h_{oe}:

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_C}\right|_{I_B \text{constant}} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}}$$

2.7 Midband analysis of BJT Single Stage Amplifiers:

Consider the basic amplifier circuit. To form a transistor amplifier only is is necessary to connect an external load and signal source along with proper biasing.

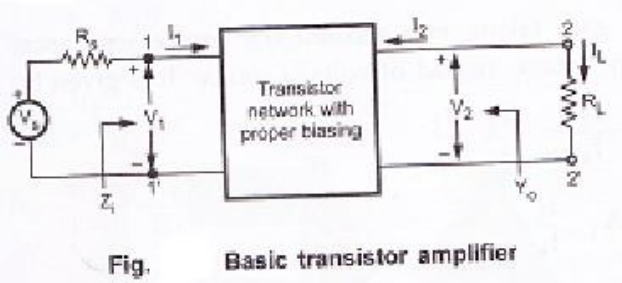


Fig. Basic transistor amplifier

We can replace the transistor circuit as shown in the following figure.

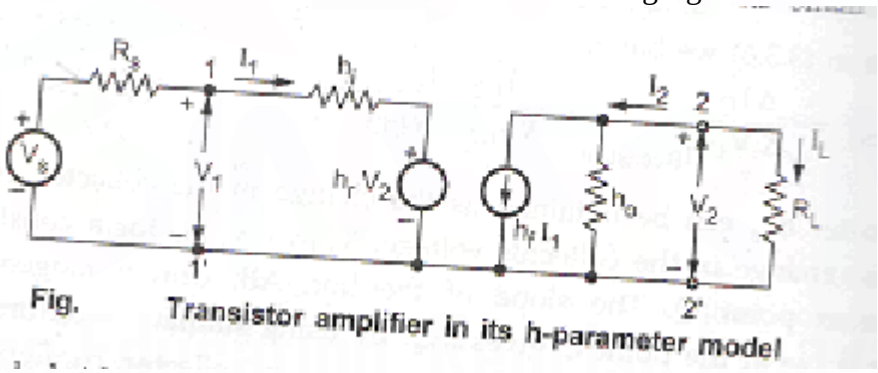


Fig. Transistor amplifier in its h-parameter model

Let us analyze the hybrid model to find current gain, input resistance, voltage gain and output resistance.

Current gain (A_i):

It is defined as the ratio of output to input current. It is given by,

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1}$$

Here I_L and I_2 are equal in magnitude but opposite in sign. $I_L = -I_2$
From above circuit,

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = -I_2 R_L$ in the equation, then equation become,

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$I_2 + h_o I_2 R_L = h_f I_1$$

$$(1 + h_o R_L) I_2 = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

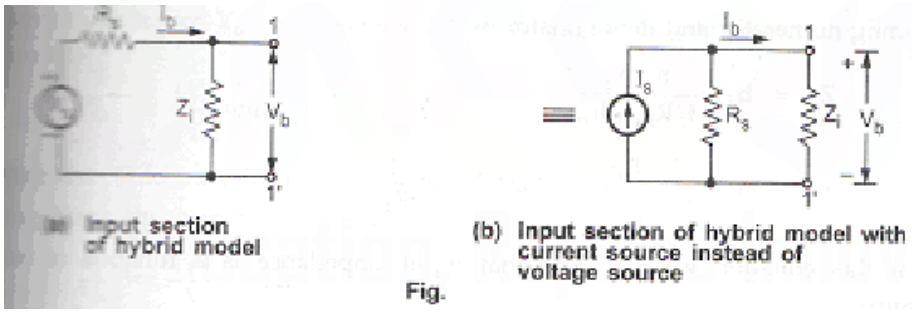
$$A_i = -\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}$$

Current gain (A_{IS}):

It is given by,

$$A_{is} = -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \cdot \frac{I_1}{I_s}$$

$$= A_i \cdot \frac{I_1}{I_s}$$



(a) Input section of hybrid model

(b) Input section of hybrid model with current source instead of voltage source

Fig.

From above figure, using current divider rule,

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$\frac{I_1}{I_s} = \frac{R_s}{Z_i + R_s}$$

$$A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

Input Impedance (Z_i):

R_i is the input resistance looking into the amplifier input terminals (1, 1'). It is given by,

$$R_i = \frac{V_1}{I_1}$$

From the input circuit,

$$V_1 = h_i I_1 + h_r V_2$$

$$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$Z_i = h_i + h_r \frac{V_2}{I_1}$$

Substituting $V_2 = -I_2R_L = A_i I_1 R_L$ in the above equation,

$$Z_i = h_i + \frac{h_r A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L$$

Substituting

$$A_i = -\frac{h_f}{1 + h_o R_L}$$

Then we get,

$$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L}$$

Dividing numerator and denominator by R_L we get,

$$Z_i = h_i - \frac{h_r h_f}{1/R_L + h_o}$$

$$Z_i = h_i - \frac{h_r h_f}{Y_L + h_o} \quad \text{where } Y_L = \frac{1}{R_L}$$

From this equation, note that the input impedance is a function offload impedance.

Voltage gain (A_v):

It is the ratio of output voltage to input voltage. It is given by,

$$A_v = \frac{V_2}{V_1}$$

By substituting $V_2 = -I_2R_L = A_i I_1 R_L$

$$A_v = \frac{A_i I_1 R_L}{V_1} = \frac{A_i R_L}{Z_i}$$

Since $\frac{I_1}{V_1} = \frac{1}{Z_i}$

Voltage gain (A_{vs}):

It is voltage gain including the source. It is given by,

$$A_{vs} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \times \frac{V_1}{V_S}$$

$$A_{vs} = A_v \times \frac{V_1}{V_S}$$

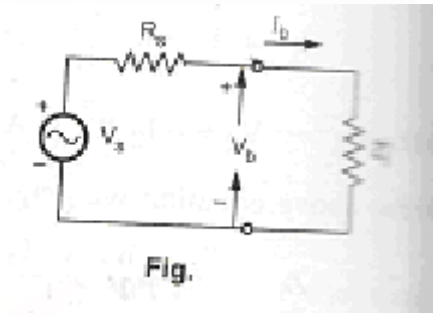


Fig.

From above figure, applying potential divider rule, then we get,

$$V_1 = \frac{Z_i}{R_s + Z_i} V_S$$

$$\frac{V_1}{V_S} = \frac{Z_i}{R_s + Z_i}$$

Substituting the value of V_1/V_s in the equation of

$$A_{vs} = A_v \times \frac{V_1}{V_S}$$

We get,

$$A_{vs} = A_v \cdot \frac{Z_i}{R_s + Z_i}$$

$$= \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i}$$

Output Admittance (Y_o):

It is the ratio of output current to output voltage. It is given by,

$$Y_o = \frac{I_2}{V_2} \text{ with } V_s = 0$$

From equation,

$$I_2 = h_f I_1 + h_o V_2$$

Dividing above equation by V_2, We get,

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$Y_o = h_f \frac{I_1}{V_2} + h_o$$

From transistor amplifier in h-parameter model circuit, with $V_s = 0$,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$
$$(R_s + h_i) I_1 = -h_r V_2$$
$$\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$

Substituting the value of I_1/V_2 from above equation in the equation of Y_o. We obtain,

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

From this equation, note that the output admittance is a function of source resistance.

Power gain (Ap):

It is the ratio of average power delivered to the load to the input power. Output power is given as,

$$P_2 = V_2 I_L = -V_2 I_2$$

Since the input power is $P_1 = V_1 I_1$

The operating power gain A_p of the transistor is given as,

$$A_p = \frac{P_2}{P_1} = -\frac{V_2 I_2}{V_1 I_1} = A_v A_i = A_i^2 \frac{R_L}{Z_i} \quad \because A_v = \frac{A_i R_L}{Z_i}$$

Relation between A_{vs} and A_{IS}:

From equation,

$A_{vs} = \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i}$ and $A_{is} = \frac{A_i R_s}{Z_i + R_s}$

We have,

$$A_{vs} = \frac{A_i R_L}{Z_i + R_s} \quad \& \quad A_{is} = \frac{A_i R_s}{Z_i + R_s}$$

Taking ratio of above two equations we get,

$$\frac{A_{vs}}{A_{is}} = \frac{R_L}{R_s}$$

$$A_{vs} = A_{is} \cdot \frac{R_L}{R_s}$$

Table: Summarizes small signal analysis of a transistor amplifier

$A_i = -\frac{h_f}{1+h_o R_L}$
$A_{is} = \frac{A_i R_s}{Z_i + R_s}$
$Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L}$
$A_v = \frac{A_i R_L}{Z_i}$
$A_{VS} = \frac{A_v R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{is} R_L}{R_s}$
$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$
$A_P = A_V A_i = A_i^2 \frac{R_L}{Z_i}$

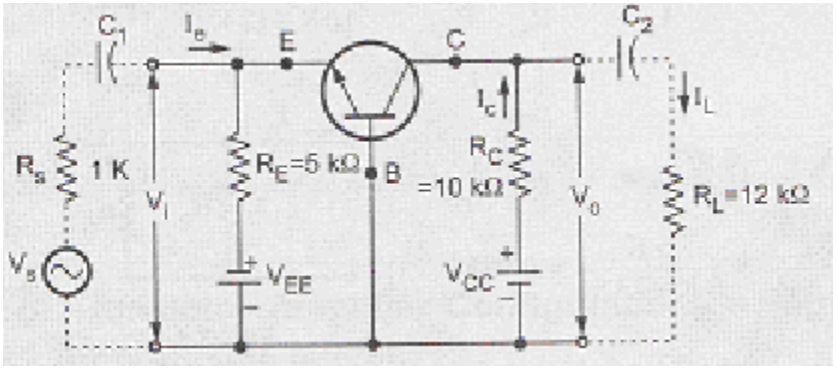
Method for analysis of a transistor circuit:

The analysis of transistor circuits for small signal behaviour can be made by following simple guidelines. These guidelines are,

1. Draw the actual circuit diagram
2. Replace coupling capacitors and emitter bypass capacitor by short circuit
3. Replace D.C. source by a short circuit
4. Mark the points B, E, C on the circuit diagram and locate these points as the start of the equivalent circuit
5. Replace the transistor by its h-parameter model

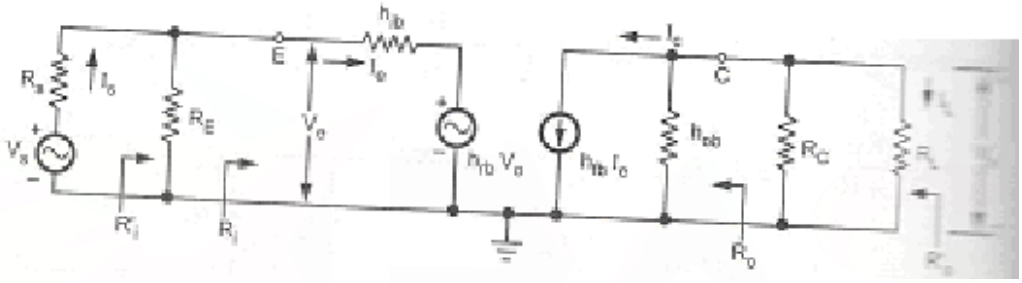
Problem 1:

For the common base circuit shown in figure, transistor parameters are $h_{ib} = 22\Omega$, $h_{fb} = -0.98$, $h_{ob} = 0.49\mu A/V$, $h_{rb} = 2.9*10^{-4}$. Calculate the values of input resistance, output resistance, current gain and voltage gain for the given circuit.



Solution:

Change the given figure into h-parameter equivalent model.



a) Current gain

$$(A_i) = -\frac{h_{fb}}{1+h_{ob}R'_L}$$

$$= \frac{-(-0.98)}{1+0.49\times10^{-6}\times5.45\ \text{K}} = \mathbf{0.977}$$

b) Input Resistance

$$(R_i) = h_{ib} + h_{rb}\ A_i\ R'_L$$

$$= 22\ \Omega + 2.9\times10^{-4}\times(0.977)\ (5.45\ \text{K}) = 23.54\ \Omega$$

$$R'_i = R_i \parallel R_E = 23.54 \parallel 5\ \text{K} = \mathbf{23.43\ \Omega}$$

c) Voltage gain

$$(A_v) = \frac{A_i R'_L}{R_i} = \frac{(0.977)\times(5.45\ \text{K})}{23.54} = \mathbf{226}$$

d) Overall voltage gain

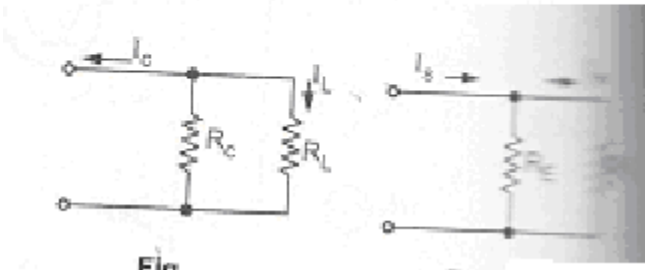
$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_e}\times\frac{V_e}{V_s} \quad \text{where } \frac{V_o}{V_e} = A_v \quad \frac{V_e}{V_s} = \frac{R'_i}{R'_i+R_s}$$

$$A_{vs} = A_v\frac{R'_i}{R'_i+R_s} = 226\times\frac{23.43}{20.36+1\ \text{K}} = \mathbf{5.174}$$

e) Overall current gain

$$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_e} \times \frac{I_e}{I_s}$$

$$\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = -\frac{10\,K}{10\,K + 12\,K} = -0.454$$



Fig

Fig.

$$\frac{I_c}{I_e} = -A_i = -0.977$$

$$\frac{I_e}{I_s} = \frac{R_E}{R_E + R_i} = \frac{5\,K}{5\,K + 23.54} = 0.995$$

$$\therefore A_{i(\text{for circuit})} = (-0.454) \times (-0.977) \times 0.996 = 0.441$$

f) Output Resistance

$$(R_o) = \frac{1}{h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_s'}}$$

$$= \frac{1}{0.49 \times 10^{-6} - \left(\frac{-0.98 \times 2.9 \times 10^{-4}}{22 + 833.33}\right)} = 1.21\ M\Omega$$

$R_o' = R_o \parallel R_L' = 1.21M \parallel 5.45K = 5.425K\Omega$

Problem 2:

Consider a single stage CE amplifier with $R_s = 1K\Omega$, $R_L = 1.2K\Omega$. Calculate A_i, R_i, A_v, A_{is}, power gain and R_o if $h_{ie} = 1.1k$, $h_{re} = 2.5*10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25\mu A/V$.

Solution:

$$A_i = \frac{-h_{fe}}{1 + h_{oe} R_L} = \frac{-50}{1 + 25 \times 10^{-6} \times 1.2 \times 10^3} = -48.54$$

$R_i = h_{ie} + h_{re} A_i R_L = 1100 - 2.5\times10^{-4} \times 48.54 \times 1200 = 1085.44\ \Omega$

$A_v = \frac{A_i R_L}{R_i} = \frac{-48.54 \times 1200}{1085.44} = -53.663$

$A_{vs} = \frac{A_v R_i}{R_i + R_s} = -\frac{53.663 \times 1085.44}{1085.44 + 1000} = -27.93$

$A_{is} = \frac{A_i R_s}{R_i + R_s} = -\frac{48.54 \times 1000}{1085.44 + 1000} = -23.28$

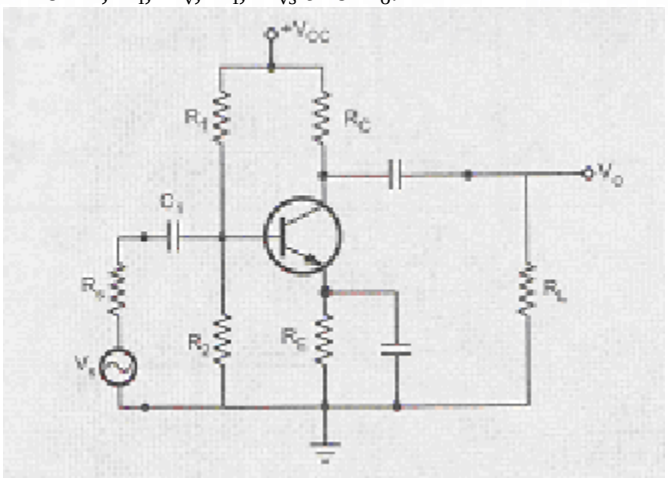
$Y_o =$ $R_o =$

$h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} = 25\times10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{1100 + 1000} = 19.0\ \mu A/V$

$\frac{1}{Y_o} = \frac{1}{19\times10^{-6}} = 52.6\ K$

Problem 3:

Consider a single stage CE amplifier with R_s = 1k, R_1 = 50k, R_2 = 2k, R_c = 2k, R_L = 2K, h_{ie} = 1.1k, h_{oe} = 25μA/V, h_{fe} = 50 and h_{re} = 2.5*10^{-4} as shown in the figure.
Find Ai, R_i, A_v, A_i, A_{vs} and R_o.



Solution:
Since h_{oe} R_L' = 25*10^{-6}*(2K || 2K) = 0.25, which is less than 0.1, so use approximate analysis.
Consider the simplified hybrid model for the given circuit.

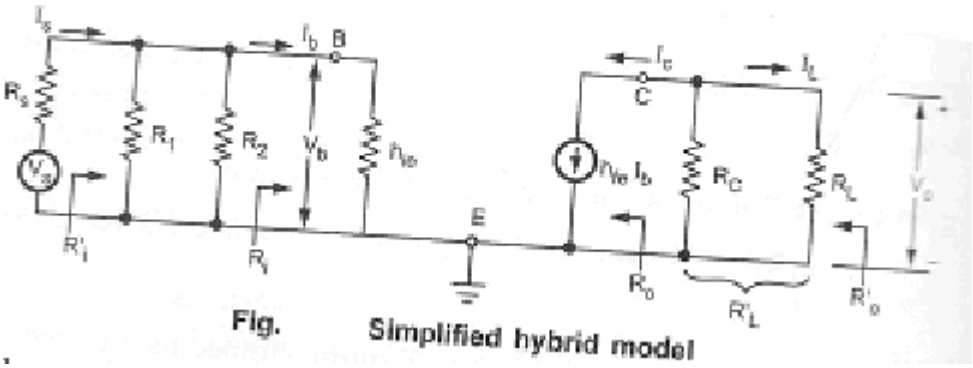


Fig. Simplified hybrid model

a) Current gain

$$(A_i) = -h_{fe} = -50$$

b) Input Impedance

$$(R_i) = h_{ie} = 1.1\ K$$

$$R'_i = h_{ie} \parallel R_1 \parallel R_2 = 1.1\ K \parallel 50\ K \parallel 2\ K = 700\ \Omega$$

c) Voltage gain

$$(A_v) = \frac{A_i R_L}{R_i} = \frac{-50 \times (2K \parallel 2K)}{1.1K} = -45.45$$

d) Output Impedance

$$(R_o) = \frac{1}{Y_o} = \infty$$

$$R'_o = R_o \parallel R'_L = \infty \parallel 2\ K \parallel 2\ K = 1\ K$$

e) Overall voltage gain

$$(A_{vs}) = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s}$$

$$A_{vs} = \frac{A_v R'_i}{R'_i + R_s} = \frac{-45.45 \times 700}{700 + 1K} = -18.71$$

f) Overall current gain

$$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

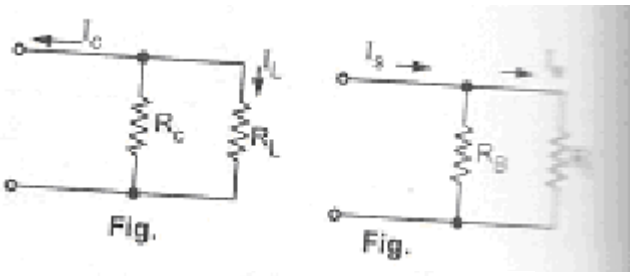


Fig. Fig.

$$\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = \frac{-1K}{1K+1K} = -0.5$$

$$\frac{I_c}{I_b} = h_{fe} = 50$$

From above figure,

$$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(50 \parallel 2)}{(50 \parallel 2)+1.1} = 0.636$$

$$A_{i\,(\text{for circuit})} = \frac{I_L}{I_s} = -0.5 \times 50 \times 0.636 = -15.9$$

Comparison of Transistor Configurations:

Sr.No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1 kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Low
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

2.8 Introduction of Differential Amplifier

A device which accepts an input signal and produces an output signal proportional to the input, is called an amplifier. An amplifier which amplifies the difference between. the two input signals is called differential amplifier. The differential amplifier configuration is used in variety of analog circuits. The. differential amplifier is an essential and basic building block in modern IC amplifier .The Integrated Circuit (IC)

technology is well known now a days, due to which the design of complex circuits become very simple. The IC version of operational amplifier is inexpensive, takes up less space and consumes less power. The. differential amplifier is the basic building block of such IC operational amplifier.

Basics of Differential Amplifier

The Differential Amplifier amplifies the difference between two input voltage signal. Hence it is also called as difference amplifier.

Consider an ideal differential amplifier shown in the Fig. A

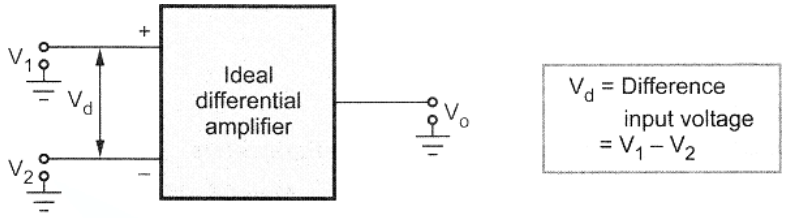


Fig. Ideal differential amplifier

V_1 and V_2 are the two input signals while Vo is the output. Each signal is measured with respect to the ground.

In an ideal differential amplifier, the output voltage Vo is proportional to the difference between the two input signals. Hence we can write,

$$V_o \propto (V_1 - V_2) \quad \ldots(1)$$

Differential Gain A_d

From Equation 1 we can write,

$$\therefore \quad V_o = A_d (V_1 - V_2) \quad \ldots(2)$$

where A_D is the constant of proportionality. The A_D is the gain with which differential amplifier amplifies the difference between two input signals. Thus it is called differential gain of the differential amplifier.

Thus, Ad = Differential gain

The difference between the two inputs (V_1 - V_2) is generally called difference voltage and denoted as Vd.

$$V_o = A_d V_d \quad \ldots(3)$$

Hence the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d} \quad \ldots(4)$$

Generally the differential gain is expressed in its decibel (dB) value as,

$$A_d = 20 \log_{10} (A_d) \text{ in dB} \quad \ldots(5)$$

Common Mode Gain Ac

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. V1 = Vz then ideally the output voltage Vo = (V_1 - V_2) A_d, must be zero.But the output voltage of the practical differential amplifier not only

depends on thedifference voltage but also depends on the average common level of the two inputs.
Such an average level of the two input signals is called common mode signal denoted as V_C

$$V_c = \frac{V_1 + V_2}{2} \quad ...(6)$$

Practically, the differential amplifier produces the output voltage proportional to such common mode signal, also. The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier $A_{C.\backslash}$

$$V_o = A_c V_c \quad ..(7)$$

Thus there exists some finite output for V1 = V2 due to such common mode gain $A_{C,}$ in case of practical differential amplifiers.

So the total output of any differential amplifier can be expressed as,

$$V_o = A_d V_d + A_c V_c \quad ..(8)$$

For an ideal differential amplifier, the differential gain A_d, must be infinite while the common mode gain must be zero.
But due to mismatch in the internal circuitry, there is some output available for V_1 = V2 and gain A_C is not practically zero. The value of such common mode gain A_C very small while the value of the differential gain A_d is always very large.

Common Mode Rejection Ratio (CMRR)

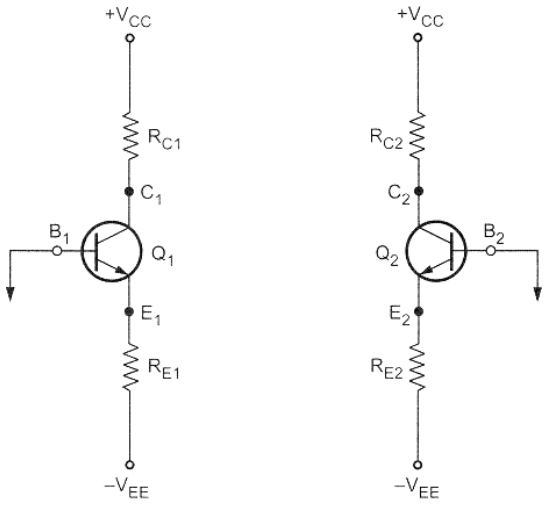
When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signal appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier. The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR. It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_C

$$\text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right| \quad ....(9)$$

$$\text{CMRR in dB} = 20 \log \left|\frac{A_d}{A_c}\right| \text{dB} \quad .....(10)$$

2.9 Transistorised Differential Amplifier

The transistorised differential amplifier basically uses the emitter biased circuits which are identical in characteristics. Such two identical emitter biased circuits are



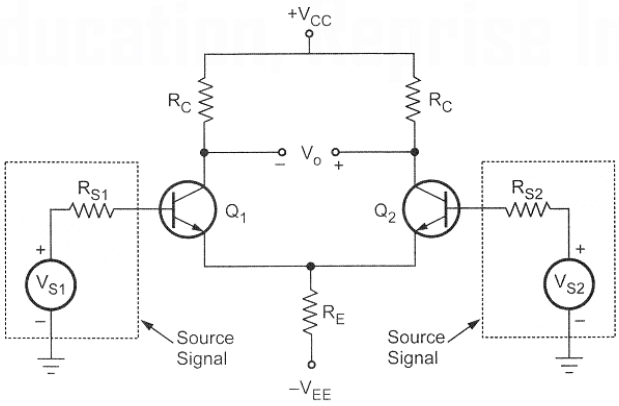
Emitter biased circuits

The two transistors Q1 and Q2 have exactly matched characteristics. The two collector
Resistors R_{C1} and R_{C2} are equal while the two emitter resistances R_{E1} and R_{E2}
are equal.

$$R_{C1} = R_{C2} \quad \text{and} \quad R_{E1} = R_{E2}$$

The magnitudes of + Vcc and – V_{EE} are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connecting emitter E1 of Q1 to the emitter E2 of Q2. Due to this, R_{E1} appears in parallel with R_{E2} and the combination can be replaced by a single resistance denoted as R_E. The base B_1 of Q1 is connected to the input 1 which is V_{S1} while the base B_2 of Q_2 is connected to the input 2 which is Vs2. The supply voltages are measured with respect to ground. The balanced output is taken between the collector C1 of Q1 and the collector C2 of Q_2. Such an amplifier is called emitter coupled differential amplifier. The two collector resistances are same hence can be denoted as R_C.

The output can be taken between two collectors or in between one of the two collectors and the ground. When the output is taken between the two collectors, none of them is grounded then it is called balanced output, double ended output or floating output. When the output is taken between any of the collectors and the ground, it is called unbalanced output or single ended output. The complete circuit diagram of such a basic dual input, balanced output differential amplifier is shown in the Fig.



Dual input, balanced output differential amplifier

As the output is taken between two output terminals, none of them is grounded, it is called balanced output differential amplifier.

Let us study the circuit operation in the two modes namely

- Differential mode operation
- Common mode operation

2.9.1 Differential Mode Operation

In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180" out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig..

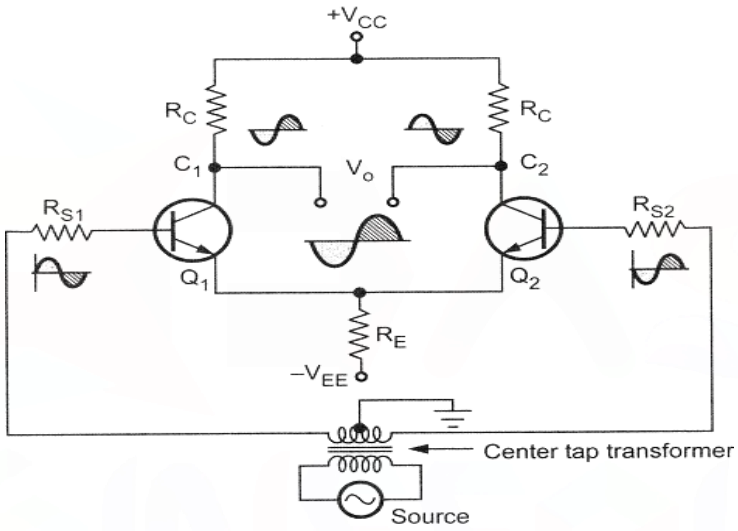


Fig Differential mode operation

Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 is negative going. With a positive going signal on the base of Q_1, m amplified negative going signal develops on the collector of Q1. Due to positive going signal, current through R_E also increases and hence a positive going wave is developed across R_E. Due to negative going signal on the base of Q2, an amplified positive going signal develops on the collector of Q_2. And a negative going signal develops across R_E, because of emitter follower action of Q_2. So signal voltages across R_E, due to the effect of Q1 and Q2 are equal in magnitude and 180o out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance. Hence R_E in this case does not introduce negative feedback. While Vo is the output taken across collector of Q1 and collector of Q_2. The two outputs on collector L and 2 are equal in magnitude but opposite in polarity. And Vo is the difference between these two signals, e.g. +10 - (-10) = + 20.

Hence the difference output Vo is twice as large as the signal voltage from either collector to ground

2.9.2 Common Mode Operation

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.

In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across R_E, which add together. Hence R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

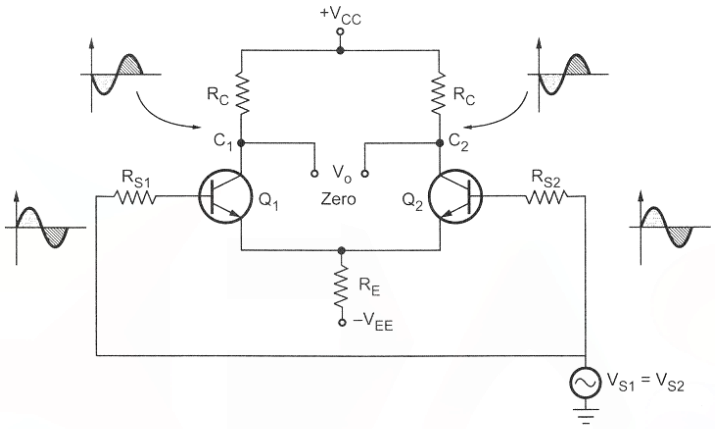


Fig. Common mode operation

While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase, Eg. (20) - (20) = 0. Thus the difference output Vo is almost zero, negligibly small. ideally it should be zero.

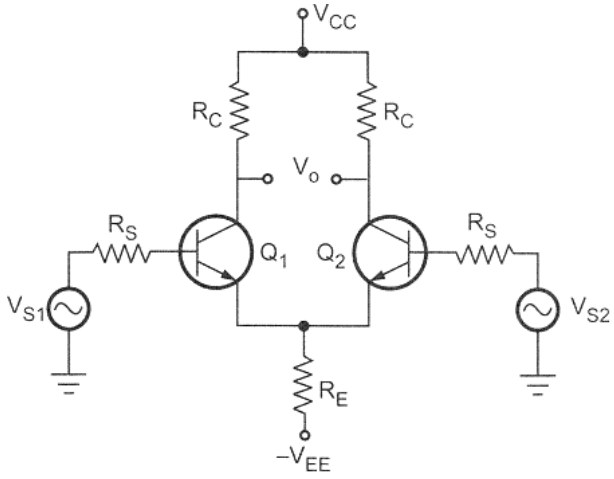
2.10 Configurations of Differential Amplifier

The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations :

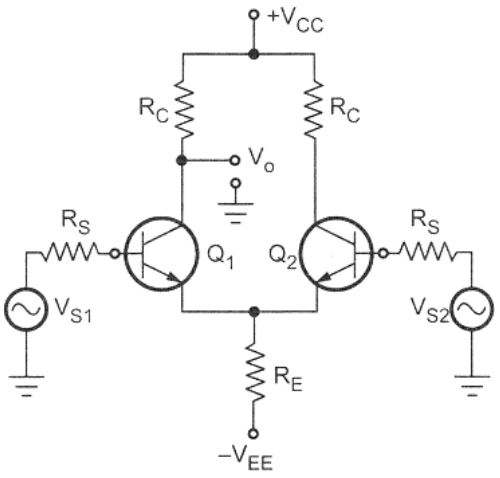
- Dual input balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier.
- Single input, balanced output differential amplifier.
- Single input, unbalanced output differential amplifier.

The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collector with respect to ground it is called unbalanced output or single ended output. If the signal is given to both the input terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input. Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Fig. (a). The dual input, unbalanced output differential amplifier is shown in the Fig.(b). The single input, balanced output

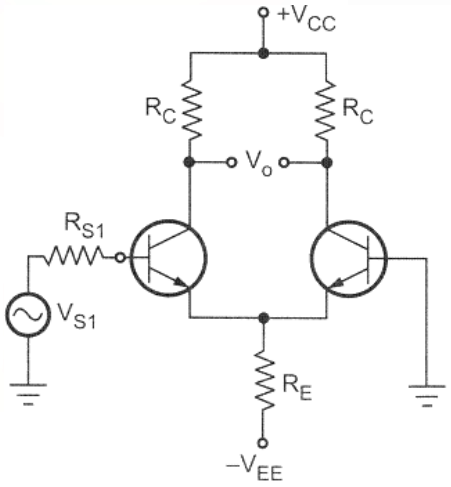
differential amplifier is shown in the Fig (c) and the single input, unbalanced output differential amplifier is shown in the Fig. (d).



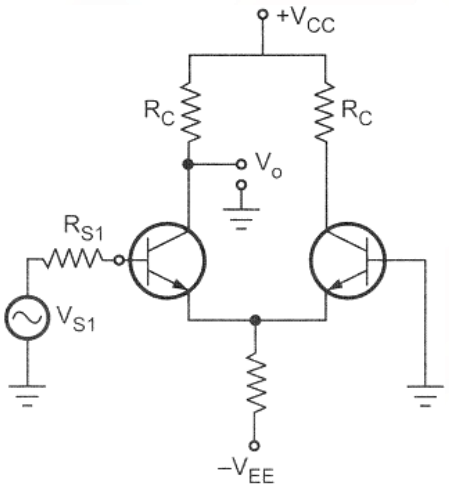
(a) Dual input balanced output



(b) Dual input unbalanced output



(c) Single input balanced output



(d) Single input unbalanced output

2.11 D.C. Analysis of Differential Amplifier

The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The d.c. equivalent circuit thus obtained is shown in the Fig.. Assuming $Rs_1 = R_{S2}$, the source resistance is simply denoted by Rs ,

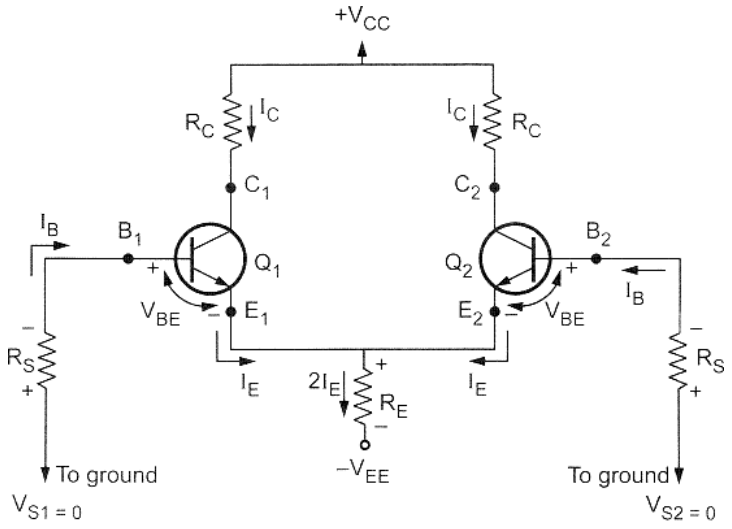


Fig. D.C. equivalent circuit

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The transistors Q1 and Q_2 are matched transistors and hence for such a matched pair we can assume :

i) Both the transistors have the same characteristics.

ii) $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \parallel R_{E2}$.

iii) $R_{C1} = R_{C2}$ hence denoted as R_C.

iv) $|V_{CC}| = |V_{EE}|$ and both are measured with respect to ground.

As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors. The same is applicable for the other transistor.

Apply-g KVL to base-emitter loop of the transistor Q1,

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots(1)$$

$$I_C = \beta I_B \text{ and } I_C \cong I_E$$

$$I_B = \frac{I_E}{\beta} \quad \ldots(2)$$

Substituting in equation (1), we get

$$\frac{-I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots(3)$$

In practice, generally $\frac{R_S}{\beta} << 2 R_E$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \quad \ldots(6)$$

Now let us determine V_{CE}. As I_E is known and $I_E \cong I_C$, we can determine the collector voltage of Q_1 as

$$V_C = V_{CC} - I_C R_C \quad \ldots(7)$$

Neglecting the drop across R_S, we can say that the voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$. Hence the collector to emitter voltage is

$$V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C \quad \ldots(8)$$

Hence $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.

Thus for both the transistors, we can determine operating point values, using equations (6) and (8) With the same biasing arrangement, the d.c. analysis remains same for all the four possible configurations of differential amplifier.

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \approx \frac{V_{EE} - V_{BE}}{2R_E} \approx I_{CQ}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

2.12 A.C. Analysis of Differential Amplifier using h-Parameters

In the a.c. analysis, we will calculate the differential gain A_d, common mode gain A_C, input resistance Ri and the output resistance R_0 of the differential amplifier circuit, using the h-parameters.

1. Differential Gain (A_d)

For the differential gain calculation, the two input signals must be different from each other. Let the two a.c. input signals be equal in magnitude but having 180" phase difference in between them. The magnitude of each a.c. input voltage V_{S1} and V_{S2} beVs /2. The two a.c. emitter currents I e_1 and I e_2 are equal in magnitude and 180' out of phase. Hence they cancel each other to get resultant a.c. current through the emitter as zero. For the a.c. purposes emitter terminal can be grounded. The a.c. small signal differential amplifier circuit with grounded emitter terminal is shown in the Fig1 As the two transistors are matched, the a.c. equivalent circuit for the other transistor is identical to the one shown in the Fig..1. Thus the circuit can be analyzed by considering only one transistor. This is called as half circuit concept of analysis. The approximate hybrid model for the above circuit can be shown as in the Fig.2, neglecting ho_e,

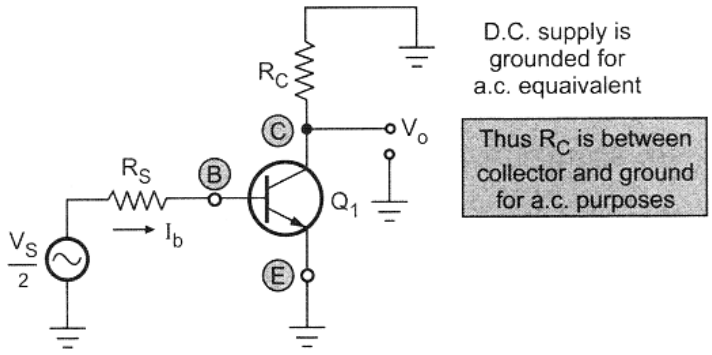


Fig. 1 A.C. equivalent for differential operation

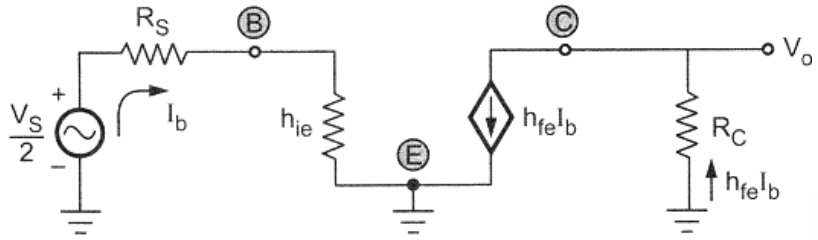


Fig. 2 Approximate hybrid model

Applying KVL to the input loop,

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \qquad \ldots(1)$$

$$-I_b(R_S + h_{ie}) = -\frac{V_S}{2}$$

$$I_b = \frac{V_S}{2(R_S + h_{ie})} \qquad \ldots(2)$$

Applying KVL to the output loop,

$$V_o = -h_{fe} I_b R_C \qquad \ldots(3)$$

Substituting equation (2) in equation (3),

$$V_o = -h_{fe} R_C \frac{V_S}{2(R_S + h_{ie})}$$

$$\frac{V_o}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \qquad \ldots(4)$$

The negative sign indicates the phase difference between input and output. Now two input signal magnitudes are V_S /2 but they are opposite in polarity, as 180" out of phase.

$$V_d = V_1 - V_2 = \frac{V_S}{2} - \left(-\frac{V_S}{2}\right) = V_S$$

The **magnitude** of the differential gain A_d is

$$A_d = \frac{V_o}{V_S} = \frac{h_{fe} R_C}{2 (R_S + h_{ie})} \quad \text{(For unbalanced output)} \qquad \ldots(5)$$

where V_S = Differential input

the expression for A_d with balanced output changes as

$$A_d = 2 \times \frac{h_{fe} R_C}{2(R_S + h_{ie})}$$

$$A_d = \frac{h_{fe} R_C}{(R_S + h_{ie})} \text{ (magnitude)} \qquad \ldots(6)$$

This is the differential gain for balanced output dual input differential amplifier circuit.

2. Common Mode Gain (A_C)

Let the magnitude of both the a.c. input signals be VS and are in phase with each other. Hence the differential input Vd = 0 while the common mode input Vc is the average value of the two.

$$V_c = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} \qquad \ldots(7)$$

$$= V_S$$

the output can be expressed as

$$V_o = A_c V_S \qquad \ldots (8)$$

$$A_c = \frac{V_o}{V_S} \qquad \ldots(8\ (a))$$

But now both the emitter currents flows through R_E in the Same direction. Hence the total current flowing through R_E is $2I_e$. considering only one transistor, as in the Fig

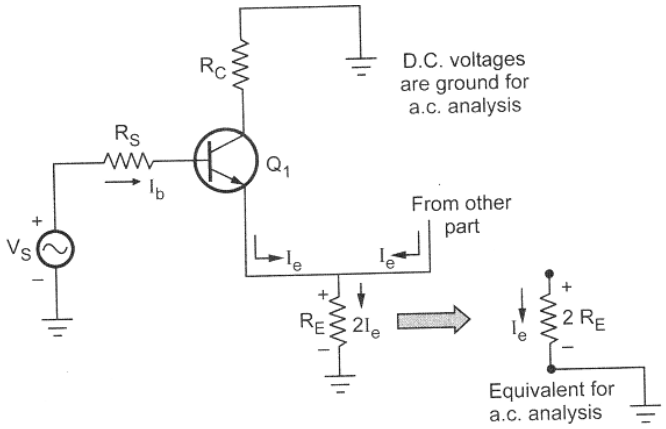


Fig. A.C. equivalent for common mode operation

The emitter resistance is shown 2 RE in the Fig

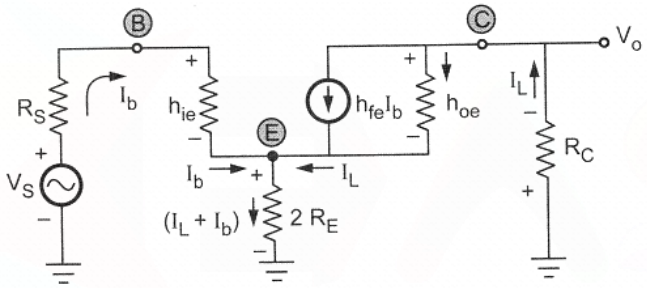


Fig. Approximate hybrid model

Current through R_C = Load current I_L

Effective emitter resistance = $2\ R_E$

Current through emitter resistance = $I_L + I_b$

Current through h_{oe} = $(I_L - h_{fe}\ I_b)$

Negative sign due to the assumed direction of current. Applying KVL to the output loop,

$$\frac{-(I_L - h_{fe}\ I_b)}{h_{oe}} - 2\ R_E\ (I_L + I_b) - I_L\ R_C = 0$$

$$\therefore \quad -\frac{I_L}{h_{oe}} + \frac{h_{fe}}{h_{oe}} I_b - 2R_E I_L - 2R_E I_b - I_L R_C = 0$$

$$I_b \left[\frac{h_{fe}}{h_{oe}} - 2R_E\right] = I_L \left[\frac{1}{h_{oe}} + 2R_E + R_C\right]$$

$$I_b [h_{fe} - 2R_E h_{oe}] = I_L [1 + h_{oe} (2R_E + R_C)]$$

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[1 + h_{oe} (2R_E + R_C)]} \quad \ldots (10)$$

Substituting value of I_b, into the equation (8(b)), we get

$$V_S = \frac{I_L[1 + h_{oe} (2R_E + R_C)](R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + I_L (2R_E)$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{[1 + h_{oe} (2R_E + R_C)](R_S + h_{ie} + 2R_E)}{[h_{fe} - 2R_E h_{oe}]} + (2R_E)$$

Finding L.C.M. and adjusting the terms, we get

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + R_S (1 + 2R_E h_{oe}) + h_{ie} (1 + 2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]}$$

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + (R_S + h_{ie}) (1 + 2R_E h_{oe}) + h_{oe} R_C [2R_E + R_S + h_{ie}]}{[h_{fe} - 2R_E h_{oe}]} \quad \ldots (11)$$

Neglecting the terms of $h_{oe} R_C$ as practically $h_{oe} R_C << 1$.

$$\therefore \quad \frac{V_S}{I_L} = \frac{2R_E (1 + h_{fe}) + (R_S + h_{ie}) (1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \quad \ldots (12)$$

Substituting the value of I_L, in the equation (9)

$$V_o = \frac{-V_S (h_{fe} - 2R_E h_{oe}) R_C}{2R_E (1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}$$

Hence the common mode gain can be written as (absorbing negative sign),

$$A_c = \frac{V_o}{V_S} = \frac{(2R_E h_{oe} - h_{fe}) R_C}{2R_E (1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \quad \ldots (13)$$

In practice h_{oe} is generally neglected hence the expression for A_c can be further modified as

$$\therefore \quad \boxed{A_c = \frac{-h_{fe} R_C}{R_S + h_{ie} + 2R_E (1 + h_{fe})}} \quad \ldots (14)$$

2.13 Common Mode rejection Ratio (CMRR)

Once the differential and common mode gains are obtained, the expression for the CMRR can be obtained as,

$$\text{CMRR} = \left|\frac{A_d}{A_c}\right|$$

$$\therefore \quad \boxed{\text{CMRR} = \frac{R_S + h_{ie} + 2R_E(1+h_{fe})}{(R_S + h_{ie})}} \qquad \ldots(15)$$

This is CMRR for **dual input balanced output** differential amplifier circuit.

2.14 Techniques of Improving Input Impedance

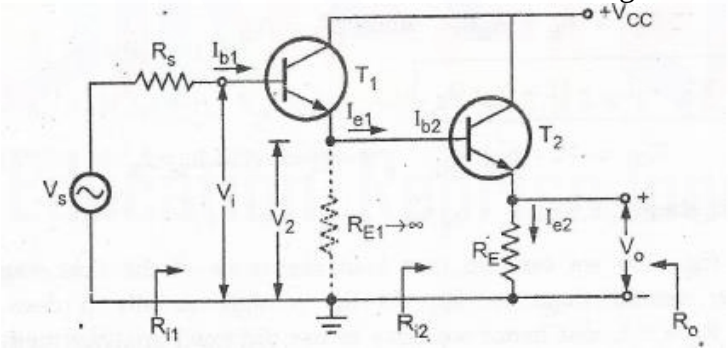
Among three configurations (CB, CC and CE), common collector or emitter follower circuit has high input impedance. Typically it is 200 KΩ to 300 KΩ. A single stage emitter follower circuit can give input impedance upto 500 KΩ. However, the input impedance considering biasing resistors is

Figure shows the direct coupling of two stages of emitter follower significantly less. Because Ri' = R_1 ll R_2 ll Ri The input impedance of the circuit can be improved by direct coupling of two stages of emitter follower amplifier. The input impedance can be increased using two techniques :

- Using direct coupling (Darlington connection)
- Using Bootstrap technique

2.14.1 Darlington Transistors

Figure shows the direct coupling of two stages of emitter follower amplifier. This cascaded connection of two emitter followers is called the Darlington connection.



Assume that the load resistance R_L is such that R_L hoe < 0.1, therefore we can use approximate analysis method for analyzing second stage.

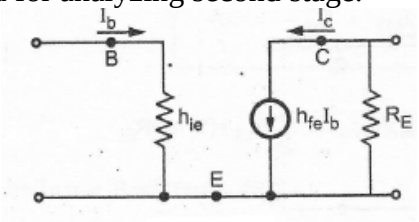
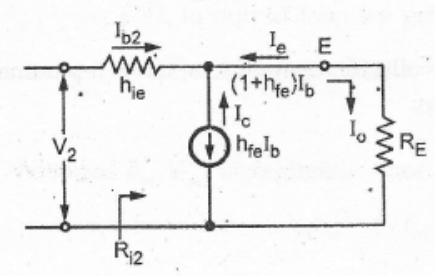


Figure shows approximate h-parameter (AC) equivalent circuit for common emitter configuration. The same circuit can be redrawn by making collector common to have approximate h-parameter equivalent circuit for common collector configuration.



Analysis of second stage :

a) Current Gain (A_{i2}) : $A_{i2} = \frac{I_o}{I_b} = -\frac{I_e}{I_b} = \frac{I_b + h_{fe} I_b}{I_b} = \frac{I_b(1+h_{fe})}{I_b}$

$\therefore$ $\boxed{A_{i2} = 1 + h_{fe}}$

b) Input Resistance (R_{i2}) : $R_{i2} = \frac{V_2}{I_{b2}}$

Applying KVL to outer loop we get,

$V_2 - I_{b2} h_{ie} - I_o R_E = 0$

$\therefore \quad V_2 = I_{b2} h_{ie} + I_o R_E$

$\therefore \quad \frac{V_2}{I_{b2}} = h_{ie} + \frac{I_o}{I_{b2}} R_E$

$\therefore \quad R_{i2} = h_{ie} + A_{i2} R_E \quad$ since, $\frac{I_o}{I_{b2}} = A_{i2}$

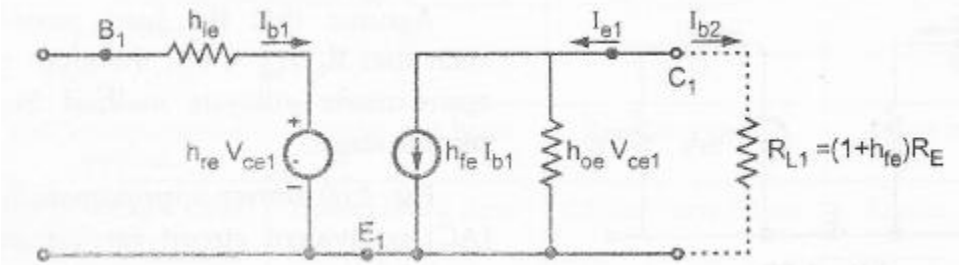
$\therefore \quad \boxed{R_{i2} = h_{ie} + (1 + h_{fe}) R_E}$

$R_{i2} = (1 + h_{fe}) R_E \quad \because h_{ie} << (1 + h_{fe}) R_E$

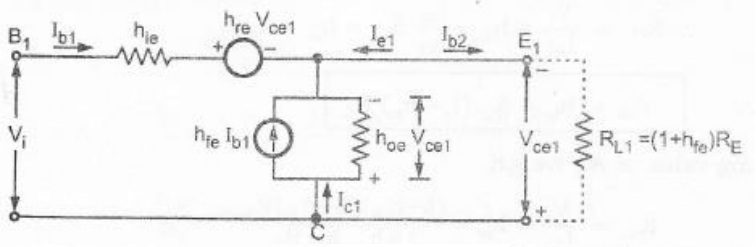
Analysis of first stage :

Load resistance of the first stage is the input resistance of the second stage i.e. R_{i2}. As R_{i2} is high, usually it does not meet the requirement hoe $R_{i2} < 0.1$, and hence we have to use the exact analysis method for analysis of the first stage.

Figure shows the h-parameter equivalent circuit for common emitter configuration.



The same circuit can be redrawn by making collector common to have h-parameter equivalent circuit for common collector for configuration.



a) Current Gain (A_{i1}) :

$$A_{i1} = \frac{I_{b2}}{I_{b1}}$$

$$A_{i1} = \frac{I_{e1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{c1})$$

and $$I_{c1} = h_{fe}I_{b1} + h_{oe}\,V_{ce1} = h_{fe}I_{b1} + h_{oe}\,(-I_{b2}\,R_{L1}) = h_{fe}I_{b1} + h_{oe}\,I_{e1}\,R_{L1}$$

Substituting value of I_{c1} equation we get,

$$\therefore \quad I_{c1} = -(I_{b1} + h_{fe}I_{b1} + h_{oe}\,I_{e2}\,R_{L1}) = -I_{b1} - h_{fe}I_{b1} - h_{oe}\,I_{e1}R_{L1}$$

$$\therefore \quad I_{e1} + h_{oe}\,R_{L1}\,I_{e1} = -I_{b1}\,(1 + h_{fe})$$

$$-\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}\,R_{L1}}$$

We know that, $R_{L1} = (1 + h_{fe})\,R_E$

$$\therefore \quad \boxed{A_{i1} = -\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}\,(1+h_{fe})\,R_E}}$$

$$= \frac{1+h_{fe}}{1+h_{oe}\,h_{fe}\,R_E} \quad \because h_{fe} >> 1$$

b) Input Resistance (R_i) : $$R_{i1} = \frac{V_i}{I_{b1}}$$

Applying KVL to output loop we get,

$$V_i - I_{b1}\,h_{ie} - h_{re}V_{ce1} + V_{ce1} = 0$$

$$\therefore V_i = I_{b1}h_{ie} + h_{re}\,V_{ce1} - V_{ce1}$$

The terms $h_{re}\,V_{ce1}$ is negligible since h_{re} is in the order of 2.5×10^{-4}

$$= I_{b1}h_{ie} - (-I_{b2}R_{L1}) = I_{b1}h_{ie} + I_{b2}R_{L1}$$

$$\therefore R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{I_{b2}}{I_{b1}}\,R_{L1} = h_{ie} + A_{i1}R_{L1}$$

$$\therefore \quad \boxed{R_{i1} = h_{ie} + A_{i1}\,(1 + h_{fe})\,R_E}$$

Substituting value of A_{i1} we get,

$$R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{(1+h_{fe})(1+h_{fe})R_E}{1+h_{oe}\,h_{fe}\,R_E}$$

$$\therefore \quad \boxed{R_{i1} = h_{ie} + \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,h_{fe}\,R_E}}$$

$$\therefore \quad \boxed{R_{i1} \approx \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,h_{fe}\,R_E}} \qquad \because h_{ie} << \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,h_{fe}\,R_E}$$

Overall current gain(Ai)

$$A_i = A_{i1} \times A_{i2}$$

$$= \frac{1+h_{fe}}{1+h_{oe}\,(1+h_{fe})\,R_E} \times (1 + h_{fe})$$

$$\therefore \quad \boxed{A_i = \frac{(1+h_{fe})^2}{1+h_{oe}\,(1+h_{fe})\,R_E}}$$

From table, we can say that Darlington connection improves input impedance as well as current gain of the circuit

Overall Voltage gain

Parameter	Single stage	Darlington
Input resistance	$R_i = (1 + h_{fe})\,R_E = 168.3\ k\Omega$	$R_i = \frac{(1+h_{fe})^2 R_E}{1+h_{oe}\,(1+h_{fe})\,R_E} = 1.65\ M\Omega$
Current gain	$A_i = 1 + h_{fe} = 51$	$A_i = \frac{(1+h_{fe})^2}{1+h_{oe}\,(1+h_{fe})\,R_E} \approx 500$

We know that

$$A_v = \frac{A_i R_L}{R_i}$$

By subtracting 1 on both sides we get

$$1 - A_v = 1 - \frac{A_i R_L}{R_i}$$

$$\therefore \quad 1 - A_v = \frac{R_i - A_i R_L}{R_i} = \frac{h_{ic} + h_{rc}\,A_i R_i - A_i R_L}{R_i}$$

$$= \frac{h_{ie}}{R_i} \quad \text{since } h_{ic} = h_{ie} \text{ and } h_{rc} = 1 - h_{re} \approx 1$$

$$\therefore \quad A_v = 1 - \frac{h_{ie}}{R_i}$$

We know that the overall voltage gain in multistage amplifier is a product of individual voltage gain

$$\therefore \quad A_v = A_{v1} A_{v2} = \left(1 - \frac{h_{ie}}{R_{i1}}\right)\left(1 - \frac{h_{ie}}{R_{i2}}\right)$$

$$\therefore \quad \boxed{A_v = 1 - \frac{h_{ie}}{R_{i2}} - \frac{h_{ie}}{R_{i1}} + \frac{h_{ie}^2}{R_{i1} R_{i2}}}$$

As we know, input resistance Ri1 >> Ri2 we can neglect term 3 and term 4 in the above equation.

$$\therefore \quad \boxed{A_v \approx 1 - \frac{h_{ie}}{R_{i2}}}$$

Output Impedance (Ro_2) :

$$R_o = \frac{1}{\text{Output admittance}} = \frac{1}{Y_o}$$

From equation, Yo of the transistor is given as

$$Y_o = Y_{o1} = h_{oc} - \frac{h_{fc} \cdot h_{rc}}{h_{ic} + R_s} = h_{oe} - \frac{-(1 + h_{fe})}{h_{ie} + R_s}$$

Since

$$h_{oc} = h_{oe,}$$

$$h_{fc} = -(1 + h_{fe})$$

And

$$h_{ic} = h_{ie}$$

$$Y_{o1} = h_{oe} + \frac{(1 + h_{fe})}{h_{ie} + R_s}$$

$$Y_{o1} = \frac{1 + h_{fe}}{h_{ic} + R_s}$$

$$\because \quad h_{oe} << \frac{(1 + h_{fe})}{h_{ic} + R_s}$$

$$\therefore \quad R_{o1} = \frac{1}{Y_{o1}}$$

$$\therefore \quad \boxed{R_{o1} = \frac{h_{ie1} + R_s}{1 + h_{fe}}}$$

Looking at Figure we can see that the R_{i1} of the first stage is the source resistance for second stage, i.e. $R_{S2} = R_{O1}$

$$\therefore \quad R_{o2} = \frac{R_{s2} + h_{ie2}}{1 + h_{fe}} = \frac{\left(\frac{h_{ie1} + R_s}{1 + h_{fe}}\right) + h_{ie2}}{1 + h_{fe}}$$

$$\therefore \quad \boxed{R_{o2} = \frac{h_{ie1} + R_s}{(1 + h_{fe})^2} + \frac{h_{ie2}}{1 + h_{fe}}}$$

Since the current in T_2 is $1+h_{fe}$ times the current in T_1, $h_{ie1} \approx (1+h_{fe})h_{ie2}$ substituting this value of h_{ie1} in equation 15 we get,

$$R_{o2} = \frac{(1+h_{fe})h_{ie2}+R_s}{(1+h_{fe})^2} + \frac{h_{ie2}}{1+h_{fe}} = \frac{h_{ie2}}{1+h_{fe}} + \frac{R_s}{(1+h_{fe})^2} + \frac{h_{ie2}}{1+h_{fe}}$$

$$\therefore \quad \boxed{R_{o2} = \frac{R_s}{(1+h_{fe})^2} + \frac{2h_{ie2}}{(1+h_{fe})}}$$

Key Point:

- In above analysis we have assumed that the h-parameter of T1 and T2 are identical,
- From the above analysis we have seen that Darlington connection of two transistorimproves current gain and input resistance of the circuit.

2.14.2 Bootstrap Emitter Follower

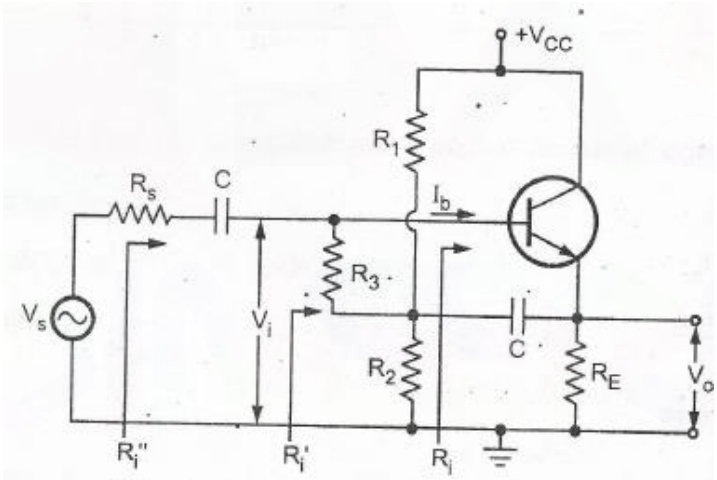


Fig. Bootstrap emitter follower

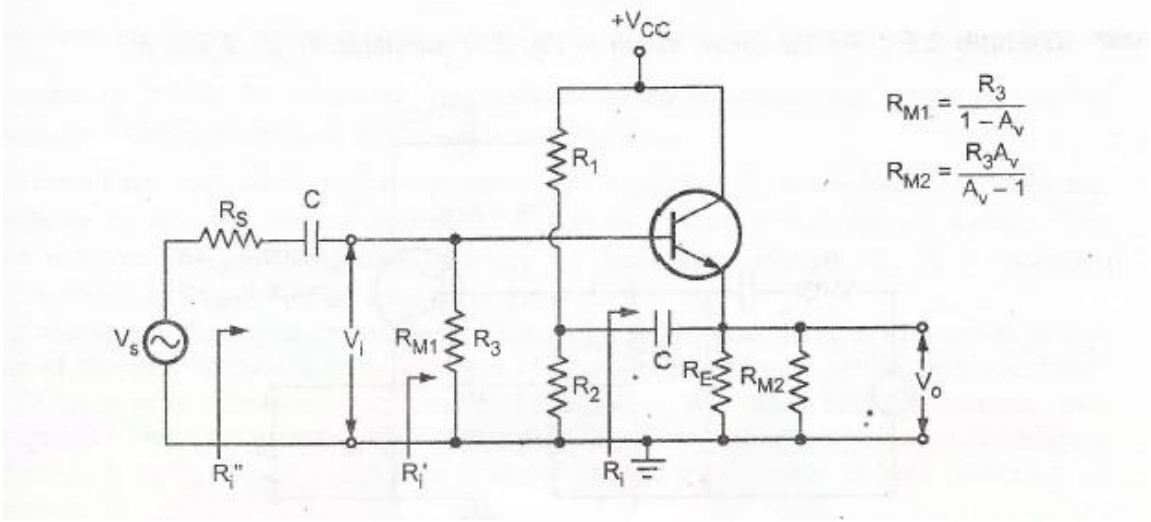
In emitter follower, the input resistance of the amplifier is reduced because of the shunting effect of the biasing resistors. To overcome this problem the emitter follower circuit is modified, as shown in the Figure. Here, two additional components are used, resistance R, and capacitor C .The capacitor, is connected between the emitter and the junction of R1,R2 and R3.

For d.c. signal, capacitor C acts as a open circuit and therefore resistance R1,R2 and R3 provides necessary biasing to keep the transistor in active region.

For ac signal, the capacitor acts as a short circuit. Its value is chosen such that it provides very low reactance nearly short circuit at lowest operating frequency. Hence for ac, the bottom of R3 is effectively connected to the output(the emitter), whereas the top of R3 is at the -input. (the base). In other words, R3 is connected between input node and output node. For such connection effective input resistance is given by Miller's theorem. The two components are

$$\frac{Z}{1-K} \quad \text{and} \quad \frac{Z \cdot K}{K-1}$$

R3 is the impedance between output voltage and input voltage and K is the voltage gain.



These are

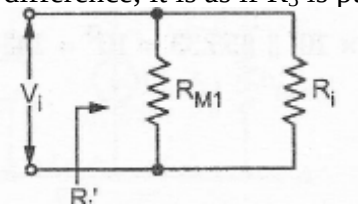
$$R_{M1} = \frac{R_3}{1-A_v} \quad \text{and} \quad R_{M2} = \frac{R_3 A_v}{A_v - 1}$$

Since, for an emitter follower, Av, approaches unity, then R_{M2} becomes extremely large.

$$R_i' = R_i \parallel R_M$$

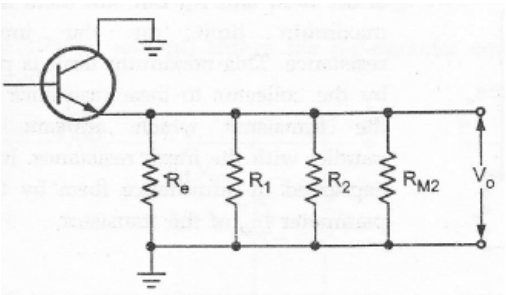
$$R_i = h_{ie} + (1 + h_{fe}) R_E$$

The above effect, when Av tends to unity is called bootstrapping. The name arises from the fact that, if one end of the resistor R_3 changes in voltage, the other end of R_3 moves through the same potential difference; it is as if R_3 is pulling itself up by its bootstraps.



The effective load on the emitter follower can be given as

$$R_{L\,eff} = R_E \parallel R_1 \parallel R_2 \parallel R_{M2}$$

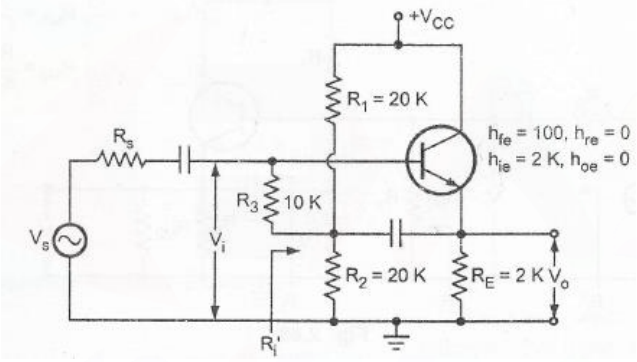


Because of the capacitor, biasing resistances R1 and R2, come on output side shunting effective load resistance. The resistance R_{M2} is very large and hence it is often neglected.

$$\therefore \quad R_{L\,eff} = R_E \parallel R_1 \parallel R_2$$

Problem

1. For the circuit shown in Figure calculate R_{Leff} , Ri, and Ri'



Solution : Here, $R_{Leff} = R_1 \parallel R_2 \parallel R_E = 20\ K \parallel 20\ K \parallel 2\ K = 1.67\ k\Omega$

$$R_i = h_{ie} + (1 + h_{fe})\, R_{L\,eff} = 2 \times 10^3 + (1 + 100) \times 1.67 \times 10^3 = 170.67\ k\Omega$$

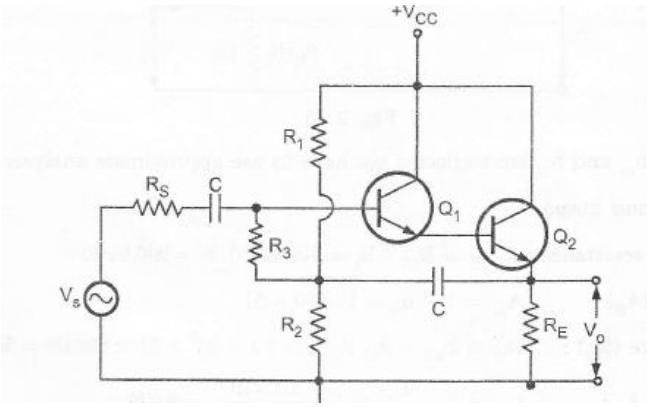
$$R_i' = R_i \parallel \frac{R_3}{1 - A_v}$$

where $$A_v = 1 - \frac{h_{ie}}{R_i} = 1 - \frac{2 \times 10^3}{170.67 \times 10^3} = 0.988$$

$$\therefore \quad R_i' = 170.67 \times 10^3 \parallel \frac{10 \times 10^3}{1 - 0.988} = 170.67 \times 10^3 \parallel 833.33 \times 10^3 = 141.66\ k\Omega$$

2. Analyze the following circuit for the following values of resistors and h-parameters

$R_s = 10\,k,\ R_1 = 100\,k,\ R_2 = 10\,k,\ R_3 = 50\,k,\ R_E = 1\,k,\ h_{ie} = 1\,k\Omega,\ h_{fe} = 100,\ h_{re} = 2.4 \times 10^{-4}$ and $h_{oe} = 2.5 \times 10^{-5}$ A/V.



Solution

Analysis of second stage

The load resistance R_{L2} for second stage is given by

$$R_{L2} = R_E \,||\, R_1 \,||\, R_2 \,||\, R_{M2}$$

By Miller's theorem R_{M2} is given as $R_{M2} = \frac{R_3 A_v}{A_v - 1}$. As A_v approaches to 1 in CC amplifier R_{M2} is very high. Hence R_{L2} can be approximated as,

$$R_{L2} = R_E \,||\, R_1 \,||\, R_2 = 1\text{ K} \,||\, 100\text{ K} \,||\, 10\text{ K} = 900.9\ \Omega$$

$$\therefore \quad h_{oe} R_{L2} = 2.5 \times 10^{-5} \times 900.9 = 0.0225$$

Since $h_{oe} R_{L2} < 0.1$ we can use the approximate analysis.

Analysis for second stage (common collector amplifier).

a) Current gain (A_{i2}) $A_{i2} = 1 + h_{fe} = 1 + 100 = 101$

b) Input resistance (R_{i2}) $R_{i2} = h_{ie} + (1 + h_{fe}) R_{L2} = 1\text{ K} + (1 + 100)\ 900.9 = 91.99\ \text{k}\Omega$

c) Voltage gain (A_{v2}) $A_{v2} = 1 - \frac{h_{ie}}{R_{i2}} = 1 - \frac{1\text{K}}{91.99\text{ K}} = 0.989$

Analysis of first stage

For first stage $R_{L1} = R_{i2} = 91.99\ \text{k}\Omega$

$$\therefore \quad h_{oe} R_{L1} = 2.5 \times 10^{-5} \times 91.99 \times 10^3 = 2.299$$

Since $h_{oe} R_{L1} > 0.1$ we have to use the exact analysis for the first stage.

a) Current gain (A_{i1}) $A_{i1} = \frac{1 + h_{fe}}{1 + h_{oe} R_{L1}} = \frac{1 + 100}{1 + [2.5 \times 10^{-5} \times 91.99 \times 10^3]} = 30.6$

b) Input resistance (R_{i1}) $R_{i1} = h_{ie} + A_{i1} R_{L1} = 1\text{K} + (30.6 \times 91.99 \times 10^3) = 2.815\ \text{M}\Omega$

c) Voltage gain (A_{v1}) $A_{V1} = 1 - \frac{h_{ie}}{R_{i1}} = 1 - \frac{1\text{K}}{2.815\text{ M}} = 0.9996$

Overall voltage gain (A_v) :

$$A_v = A_{v1} \times A_{v2} = 0.9996 \times 0.989 = 0.988$$

Overall input resistance (R_i) :

$$R_i = R_{i1} \,||\, R_{M1} \qquad \text{where} \quad R_{M1} = \frac{R_3}{1 - A_v} = \frac{50\,K}{1 - 0.988} = 4.166\ M\Omega$$

$$\therefore \quad R_i = 2.815\ M \,||\, 4.166\ M = 1.679\ M\Omega$$

Overall voltage gain (A_{vs}) :

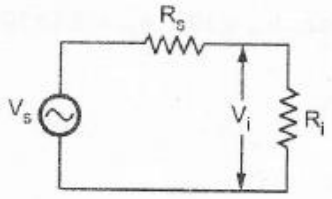


Fig. 2.79

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}$$

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

$$= A_v \times \frac{R_i}{R_i + R_s}$$

$$= 0.988 \times \frac{1.679\,M}{1.679\,M + 10\,K} = 0.982$$

Output resistance (R_o) :

$$R_{o1} = \frac{R_{s1} + h_{ie}}{1 + h_{fe}} \qquad \text{where } R_{s1} = R_{M1} || R_s = 4.166\ M \,||\, 10\ K = 9.976\ K$$

$$= \frac{9.976\,K + 1\,K}{1 + 100} = 108.6\ \Omega$$

$$R_{o2} = \frac{R_{s2} + h_{ie}}{1 + h_{fe}} = \frac{R_{o1} + h_{ie}}{1 + h_{fe}} \qquad \because R_{s2} = R_{o1}$$

$$= \frac{108.6 + 1K}{1 + 100} = 10.976\ \Omega$$

$$R_o = R_{o2} = R_{L2} = 10.976 \,||\, 900.9 = 10.84\ \Omega$$

Multistage Amplifiers

In practice, we need amplifier which can amplify a signal from a very weak source such as a microphone, to a level which is suitable for the operation of another transducer such as loudspeaker . This is achieved by cascading number of amplifier stages, known as multistage amplifier

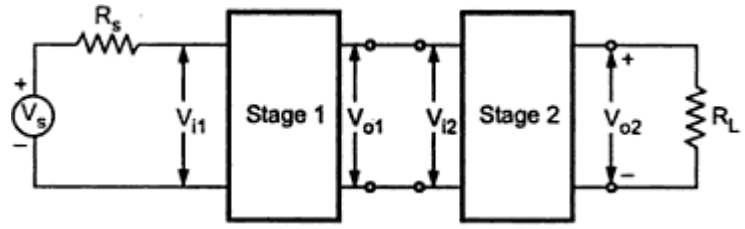
Need for Cascading

For faithful amplification amplifier should have desired voltage gain, current gain and it should match its input impedance with the source and output impedance with the load. Many times these primary requirements of the amplifier can not be achieved with single stage amplifier, because of the limitation of the transistor/FET parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.

We can say that,

- When the amplification of a single stage amplifier is not sufficient, or,
- When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier,with two or more stages is also known as multistage amplifier.

Two Stage Cascaded Amplifier



Vi1 is the input of the first stage and Vo2 is the output of second stage.
So,Vo2/Vi1 is the overall voltage gain of two stage amplifier.

$$A_V = \frac{V_{o2}}{V_{i1}}$$

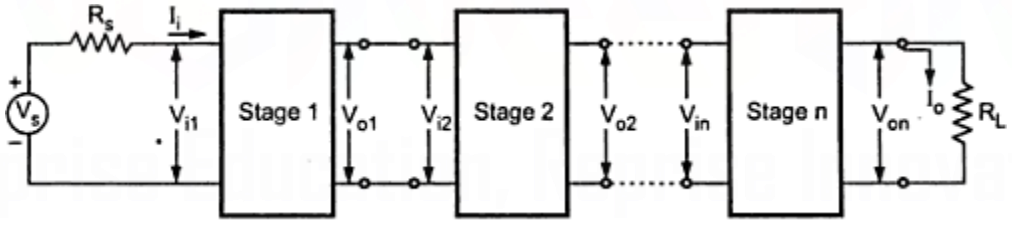
$$= \frac{V_{o2}}{V_{i2}} \frac{V_{i2}}{V_{i1}}$$

$$V_{o1} = V_{i2}$$

$$\therefore A_V = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}}$$

$$= A_{V2} A_{V1}$$

n-Stage Cascaded Amplifier



Voltage gain :
The resultant voltage gain of the multistage amplifier is the product of voltage gains of the various stages.
Av = Avl Av2 ... Avn
Gain in Decibels
In many situations it is found very convenient to compare two powers on logarithmic scale rather than on a linear scale. The unit of this logarithmic scale is called decibel (abbreviated dB). The number N decibels by which a power P2 exceeds the power P1 is defined by

$$N = 10 \log \frac{P_2}{P_1}$$

Decibel, dB denotes power ratio. Negative values of number of dB means that the power P2 is less than the reference power P1 and positive value of number of dB means the power P2 is greater than the reference power P1.
For an amplifier, P1 may represent input power, and P2 may represent output power.
Both can be given as

$$P_1 = \frac{V_i^2}{R_i} \text{ and } P_2 = \frac{V_o^2}{R_o}$$

Where Ri and Ro are the input and output impedances of the amplifier respectively.Then,

$$N = 10 \log_{10} \frac{V_o^2 / R_o}{V_i^2 / R_i}$$

If the input and output impedances of the amplifier are equal i.e. Ri = Ro= R, then

$$N = 10 \log_{10} \frac{V_o^2}{V_i^2} = 10 \log_{10} \left(\frac{V_o^2}{V_i^2} \right) = 10 \times 2 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{V_o}{V_i}$$

Gain of Multistage Amplifier in dB

The gain of a multistage amplifier can be easily calculated if the gain of the individual stages are known in dB, as shown below

$20 \log_{10} Av = 20 \log_{10} Avl + 20 \log_{10} Av2 + \ldots + 20 \log_{10} Avn$

Thus, the overall voltage gain in dB of a multistage amplifier is the decibel voltage gains of the individual stages. It can be given as

AvdB = AvldB + Av2dB + ... + AvndB

Advantages of Representation of Gain in Decibels

Logarithmic scale is preferred over linear scale to represent voltage and power gains because of the following reasons :

- In multistage amplifiers, it permits to add individual gains of the stages to calculate overall gain.
- It allows us to denote, both very small as well as very large quantities of linear, scale by considerably small figures.

  For example, voltage gain of 0.0000001 can be represented as -140 dB and voltage gain of 1,00,000 can be represented as 100 dB.
- Many times output of the amplifier is fed to loudspeakers to produce sound which is received by the human ear. It is important to note that the ear responds to the sound intensities on a proportional or logarithmic scale rather than linear scale. Thus use of dB unit is more appropriate for representation of amplifier gains.

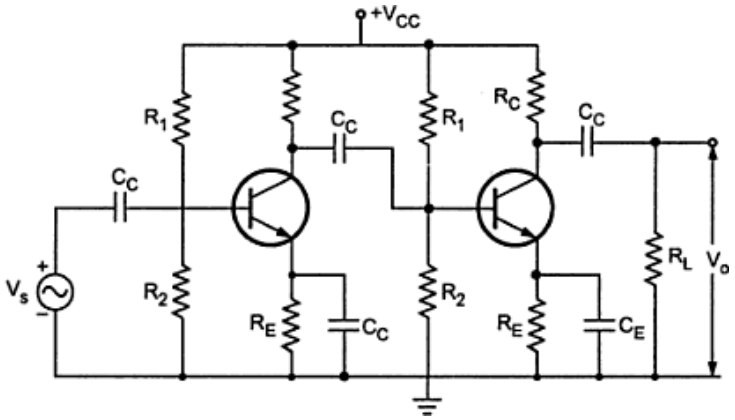
Methods of coupling Multistage Amplifiers

In multistage amplifier, the output signal of preceding stage is to be coupled to the input circuit of succeeding stage. For this interstage coupling, different types of coupling elements can be employed. These are :

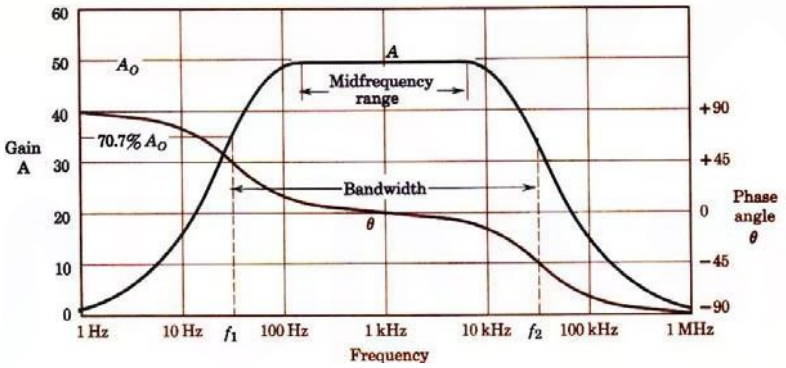
1. RC coupling 2. Transformer coupling 3. Direct coupling

RC coupling

Figure shows RC coupled amplifier using transistors. The output signal of first stage is coupled to the input of the next stage through coupling capacitor and resistive load at the output terminal of first stage

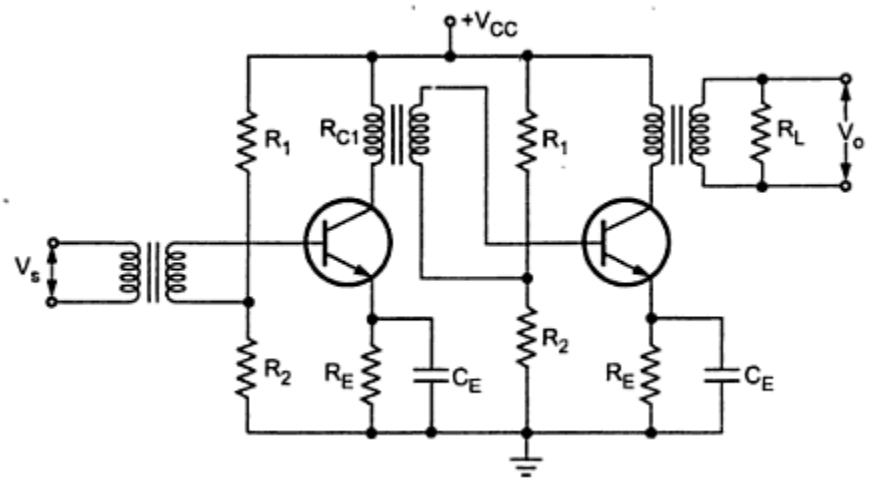


The coupling does not affect the quiescent point of the next stage since the coupling capacitor Cc blocks the d.c. voltage of the first stage from reaching the base of the second stage. The RC network is broadband in nature. Therefore, it gives a wideband frequency response without peak at any frequency and hence used to cover a complete A.F amplifier bands. However its frequency response drops off at very low frequencies due to coupling capacitors and also at high frequencies due to shunt capacitors such as stray capacitance.

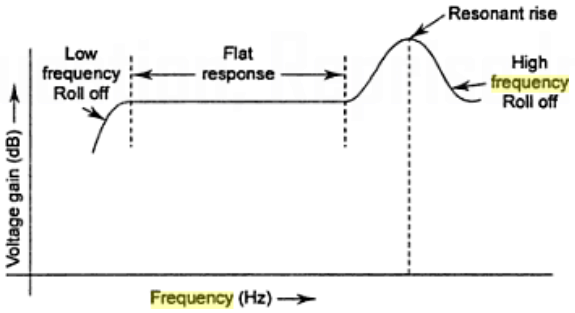


Transformer Coupling

Figure shows transformer coupled amplifier using transistors. The output signal of first stage is coupled to the input of the next stage through an impedance matching transformer

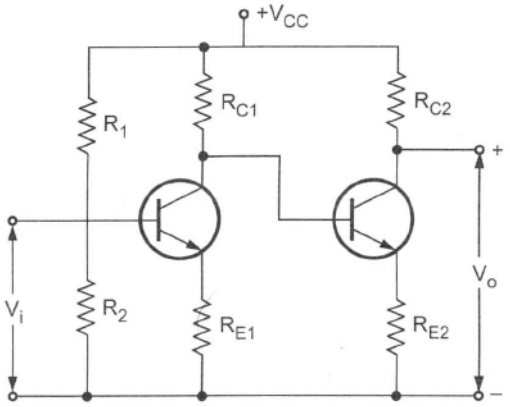


This type of coupling is used to match the impedance between output and input cascaded stage. Usually, it is used to match the larger output resistance of AF power amplifier to a low impedance load like loudspeaker. As we know, transformer blocks d.c, providing d.c. isolation between the two stages. Therefore, transformer coupling does not affect the quiescent point of the next stage. Frequency response of transformer coupled amplifier is poor in comparison with that an RC coupled amplifier. Its leakage inductance and inter winding capacitances does not allow amplifier to amplify the signals of different frequencies equally well. Inter winding capacitance of the transformer coupled may give rise resonance at certain frequency which makes amplifier to give very high gain at that frequency. By putting shunting capacitors across each winding of the transformer, we can get resonance at any desired RF frequency. Such amplifiers are called tuned voltage amplifiers. These provide high gain at the desired of frequency, i.e. they amplify selective frequencies. For this reason, the transformer-coupled amplifiers are used in radio and TV receivers for amplifying RF signals. As d.c. resistance of the transformer winding is very low, almost all d.c. voltage applied by Vcc is available at the collector. Due to the absence of collector resistance it eliminates unnecessary power loss in the resistor.



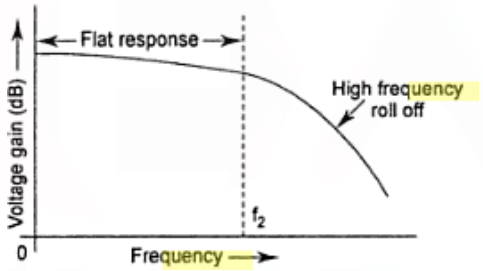
Direct Coupling

Figure shows direct coupled amplifier using transistors. The output signal of first stage is directly connected to the input of the next stage. This direct coupling allows the quiescent d.c. collector current of first stage to pass through base of the next stage, affecting its biasing conditions.



Due to absence of RC components, frequency response is good but at higher frequencies shunting capacitors such as stray capacitances reduce gain of the amplifier.

The transistor parameters such as V_{BE} and β change with temperature causing the collector current and voltage to change. Because of direct coupling these changes appear at the base of next stage, and hence in the output. Such an unwanted change in the output is called drift and it is serious problem in the direct coupled amplifiers.



Example : *An op-amp has a differential gain of 80 dB and CMRR of 95 dB. If $V_1 = 2\mu V$ and $V_2 = 1.6\ \mu V$, then calculate the differential and common mode output values.*

Solution : A_d = 80 dB and CMRR = 95 dB

Do not use dB values for the calculation directly.

A_d in dB = 20 log A_d

$\therefore$ 80 = 20 log A_d

$\therefore$ $A_d = 1 \times 10^4$ (absolute)

CMRR in dB = 20 log CMRR

$$\therefore \quad 95 = 20 \log CMRR$$

$$\therefore \quad CMRR = 5.6234 \times 10^4$$

$\therefore$ Differential output can be calculated as

$$V_d = A_d (V_1 - V_2) = 1 \times 10^4 (2 - 1.6) \times 10^{-6}$$

$$= \mathbf{4\ mV}$$

And common mode output can be calculated as,

$$V_c = A_c \frac{(V_1 + V_2)}{2}$$

Now $$CMRR = \frac{A_d}{A_c}$$

$$\therefore \quad 5.6234 \times 10^4 = \frac{1 \times 10^4}{A_c}$$

$$\therefore \quad A_c = 0.1778$$

$$\therefore \quad V_c = 0.1778 \times \frac{(2 + 1.6)}{2} \times 10^{-6}$$

$$= \mathbf{0.32\ \mu V}$$

➠ **Example :** *The common mode input to a certain differential amplifier, having differential gain of 125 is 4 sin 200 π t V. Determine the common mode output if CMRR is 60 dB.*

Solution : The CMRR in dB is

$$60 = 20 \log \left| \frac{A_d}{A_c} \right|$$

Hence the common mode output is

$$= A_c V_c = 0.125 (4 \sin 200 \pi t)$$

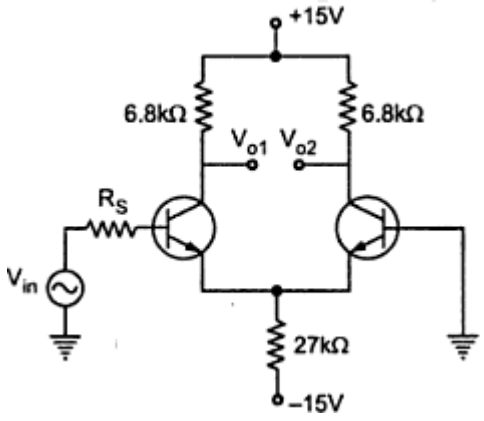
$$= \mathbf{0.5 \sin (200 \pi t)\ V}$$

➠ **Example :** *For the differential amplifier shown in the Fig. determine*

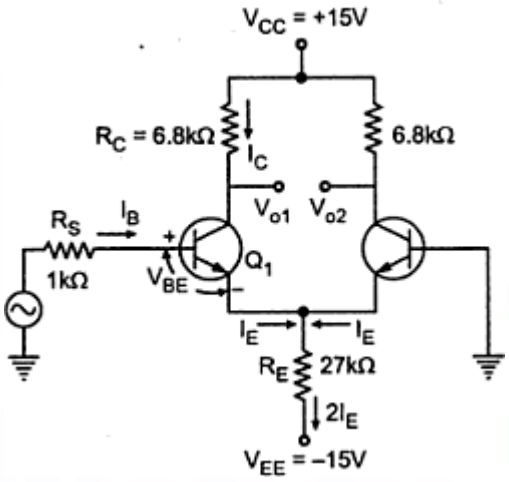
i) The voltages at the collector of each transistor

ii) The differential voltage gain.

Assume V_{BE} = 0.7 V, h_{fe} =100, h_{ie} = 3.9 kΩ and the source resistance as 1 kΩ.



Solution : The circuit is redrawn showing the various voltages and current



i) Applying KVL to the base emitter loop of Q_1,

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0$$

Now $$I_B = \frac{I_E}{\beta} \text{ where } \beta = h_{fe}$$

$$\therefore \quad \frac{-I_E R_S}{\beta} - V_{BE} - 2I_E R_E + V_{EE} = 0$$

$$\therefore \quad I_E \left[\frac{R_S}{\beta} + 2R_E\right] + V_{BE} - V_{EE} = 0$$

$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} = \frac{15 - 07}{\frac{1 \times 10^3}{100} + 2 \times 27 \times 10^3}$$

$$= 0.264 \text{ mA}$$

$$\therefore \quad I_C = I_E = 0.264 \text{ mA}$$

$$\therefore \quad V_{o1} = V_{o2} = V_{CC} - I_C R_C$$

$$= 15 - 0.264 \times 10^{-3} \times 6.8 \times 10^3$$

$$= \mathbf{13.2\ V}$$

QUESTIONS

2 MARKS

1. What are the advantages of Darlington amplifier?
2. Explain Miller's theorem. (May/jun 2103)
3. What are the limitations of h parameters?
4. What are practical limitations in selecting very high R_E?
5. Define i) Differential gain ii) Common mode gain
6. State Miller's Theorem. (May,15)
7. How can a DC equivalent circuit of an amplifier be obtained?
8. Draw the Darlington emitter follower circuit. (May,14,13)
9. What does bootstrapping mean? Why bootstrapping is done in a buffer amplifier?
10. Define Common Mode Rejection Ratio. (Nov,09)
11. What is the coupling schemes used in multistage amplifiers? (May,10)
12. What are the advantages of Representation of Gain in Decibels.
13. What is the typical value of CMRR? How the constant current circuit is used to improve the CMRR? (Nov,14)
14. Find the value of αdc when Ic=8.2mA and Ie=8.7mA.
15. What are the advantages of h-parameters? (Nov,14)
16. What is the role of coupling network in multistage amplifiers?
17. Define voltage & current gain of an emitter follower.
18. Why CE amplifier better than CC & CB amplifiers?
19. What is the difference between cascade and cascode amplifier?
20. Mention two importance characteristics of CC circuit.
21. State Bisection Theorem. (Nov,12)
22. Draw the small signal equivalent circuit of CE amplifier.
23. If CMMR of amplifier is 100dB, calculate CM gain if difference gain is1000.
24. Two identical amplifiers are cascaded, having 10dBgain each other. Calculate output voltage if the input of 1mv

16 MARKS

1. Draw a CE amplifier & its small signal equivalent. Derive its Avs, Ai, Rin, Ro.
2. For the CC amplifier circuit, Find the expressions for input impedance and voltage gain. Assume suitable model for transistor.
3. Explain with circuit diagram of Darlington connection and derive the expression for Ai, Av, Ri &Ro.
4. Explain the emitter coupled differential amplifier with neat diagram & Derive expression for CMRR.
5. Discuss transfer characteristics of differential amplifier. Explain the methods used to improve CMRR.
6. Derive the expressions for the common mode and differential mode gains of a differential amplifier in terms of h-parameters.
7. Compare CE, CB, CC amplifiers.
8. Derive the expressions for the voltage gain, current gain, input and output impedance of emitter follower amplifier.
9. Derive expression for voltage gain of CS & CD amplifier under small signal low frequency condition.
10. Draw a two stage RC coupled amplifier and explain. Compare cascade and cascode amplifier?
11. Consider a single stage CE amplifier with Rs=1kΩ, R1=50KΩ, R2=2KΩ, RC=2KΩ, RL=2KΩ, hfe=50, hie=1.1 KΩ, hoe=25μmho, hre=2.5×10-4. Find Ai,Ri,Av,Ais,Avs and R0.
12. The Darlington amplifier has the following parameters, Rs=3kΩ, RE=3kΩ, hie=1.1 KΩ, hfe=50, hre=2.5×10-4, hoe=25μmho. Then calculate Ai, Ri, Av and R0.
13. The dual input balanced output differential amplifier having Rs=100Ω, RC=4.7KΩ, RE=6.8KΩ, hfe=100, Vcc=+15v and VEE=-15v. Calculate operating point values, differential & common mode gain, CMRR, and output if VS1= 70mV(p-p) at 1 KHz & VS2= 40mV(p-p) at 1 KHz