JEPPIAAR INSTITUTE OF TECHNOLOGY

"Self-Belief | Self Discipline | Self Respect"

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE NOTES

EC8351 – ELECTRONIC CIRCUITS 1

(Regulation 2017)

Year/Semester: II/03

2021 – 2022

Prepared by

Ms.S.SUREKHA

Assistant Professor/ECE

SYLLABUS

EC8351 **ELECTRONIC CIRCUITS 1** **L T P C 3 0 0 3**

OBJECTIVES:

- To understand the methods of biasing transistors
- To design and analyze single stage and multistage amplifier circuits
- To analyze the frequency response of small signal amplifiers
- To design and analyze the regulated DC power supplies.
- To troubleshoot and fault analysis of power supplies

UNIT I BIASING OF DISCRETE BJT, JFET AND MOSFET

BJT– Need for biasing — DC Load Line and Bias Point — DC analysis of Transistor circuits — Various biasing methods of BJT — Bias Circuit Design — Thermal stability — Stability factors — Bias compensation techniques using Diode, thermistor and sensistor — Biasing BJT Switching Circuits- JFET — DC Load Line and Bias Point — Various biasing methods of JFET — JFET Bias Circuit Design — MOSFET Biasing — Biasing FET Switching Circuits.

UNIT II BJT AMPLIFIERS

Small Signal Hybrid p equivalent circuit of BJT — Early effect — Analysis of CE, CC and CB amplifiers using Hybrid p equivalent circuits — AC Load Line Analysis- Darlington Amplifier — Bootstrap technique — Cascade, Cascode configurations — Differential amplifier, Basic BJT differential pair — Small signal analysis and CMRR.

UNIT III SINGLE STAGE FET, MOSFET AMPLIFIERS

Small Signal Hybrid p equivalent circuit of FET and MOSFET — Analysis of CS, CD and CG amplifiers using Hybrid p equivalent circuits — Basic FET differential pair- BiCMOS circuits.

UNIT IV FREQUENCY RESPONSE OF AMPLIFIERS

Amplifier frequency response — Frequency response of transistor amplifiers with circuit capacitors — BJT frequency response — short circuit current gain — cut off frequency — fa, fß and unity gain bandwidth — Miller effect — frequency response of FET — High frequency analysis of CE and MOSFET CS amplifier — Transistor Switching Times.

UNIT V POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

Linear mode power supply — Rectifiers — Filters — Half-Wave Rectifier Power Supply — Full- Wave Rectifier Power Supply — Voltage regulators: Voltage regulation — Linear series, shunt and switching Voltage Regulators — Over voltage protection — BJT and MOSFET — Switched mode power supply (SMPS) — Power Supply Performance and Testing — Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

TOTAL: 45 PERIODS

OUTCOMES:

After studying this course, the student should be able to:

- Acquire knowledge of ♣Working principles, characteristics and applications of BJT and FET♣Frequency response characteristics of BJT and FET amplifiers
- Analyze the performance of small signal BJT and FET amplifiers - single stage and multi stage amplifiers
- Apply the knowledge gained in the design of Electronic circuits

TEXT BOOKS:

1. Donald. A. Neamen, Electronic Circuits Analysis and Design, 3rd Edition, Mc Graw Hill Education (India) Private Ltd., 2010. (Unit I-IV)
2. Robert L. Boylestad and Louis Nasheresky, ―Electronic Devices and Circuit Theory‖, 11thEdition, Pearson Education, 2013. (Unit V)

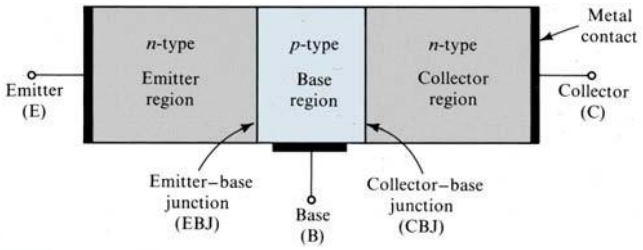
REFERENCES

1. Millman J, Halkias.C.and Sathyabrada Jit, Electronic Devices and Circuits, 4th Edition, Mc Graw Hill Education (India) Private Ltd., 2015.
2. Salivahanan and N. Suresh Kumar, Electronic Devices and Circuits, 4th Edition, , Mc Graw Hill Education (India) Private Ltd., 2017.
3. Floyd, Electronic Devices, Ninth Edition, Pearson Education, 2012.
4. David A. Bell, Electronic Devices & Circuits, 5th Edition, Oxford University Press, 2008.
5. Anwar A. Khan and Kanchan K. Dey, A First Course on Electronics, PHI, 2006.
6. Rashid M, Microelectronics Circuits, Thomson Learning, 2007

UNIT I

1.1 Introduction

BJT consists of 2 PN junctions. It has three terminals: emitter, base and collector. Transistorcan be operated in three regions, namely cut-off, active and saturation by applying proper biasing conditions.



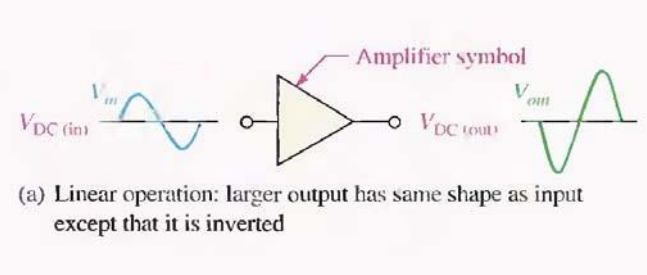
Region of Operation	Emitter Base Junction	Collector Base Junction
Cut-off	Reverse biased	Reverse biased
Active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased

- Active:
  - Most important mode, e.g. for amplifier operation and switching application
  - The region where current curves are practically flat.
- Saturation:
  - Barrier potential of the junctions cancels each other out causing a virtual short.
  - Ideal transistor behaves like a closed switch.
- Cutoff:
  - Current reduced to zero
  - Ideal transistor behaves like an open switch.

In order to operate transistor in the desired region we have to apply external d.c. voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor.

When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or d.c. operating point or quiescent point. The operating point must be stable for proper operation of the transistor. However, the operating point shifts with changes in transistor parameters such as β, Ico and V_{BE}. As transistor parameters are temperature dependent, the operating point also varies with changes in temperature.

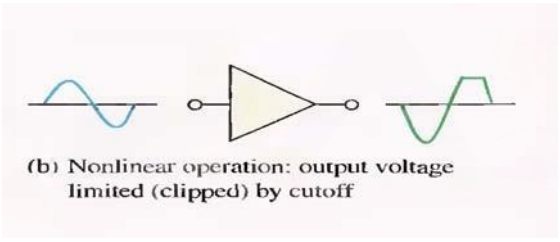
1.2 Need for biasing



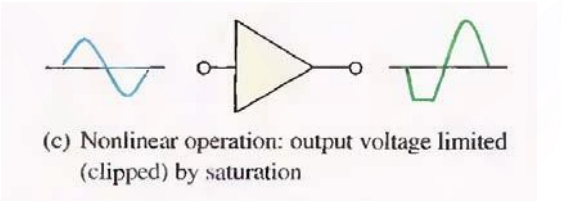
(a) Linear operation: larger output has same shape as input except that it is inverted

Fig.1.1 (a)

Bias establishes the DC operating point for proper linear operation of an amplifier. If an amplifier is not biased with correct DC voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 1.1 shows the effects of proper and improper DC biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180^0 out of phase with the input. The output signal swings equally above and below the dc bias level of the output, $V_{DC(out)}$.



(b) Nonlinear operation: output voltage limited (clipped) by cutoff



(c) Nonlinear operation: output voltage limited (clipped) by saturation

Fig.1.1 (b), (c)

Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff.
Part (c) shows limiting of the negative portion of the output voltage as a result of a de operating point being too close to saturation.

1.3 Load line and Variation of quiescent point

Biasing is the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point). The operating point of a device, also known as bias

point, quiescent point, or Q-point, is the point on the output characteristics that shows the DC collector–emitter voltage (V_{ce}) and the collector current (I_c) with no input signal applied.

Consider the fixed bias circuit,

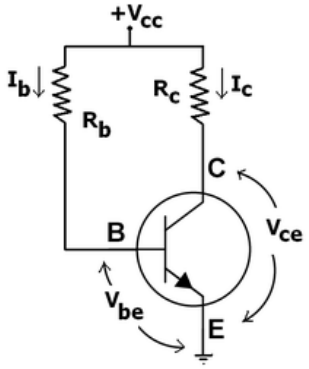


Fig 1.2

We have,

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \left[\frac{1}{R_C}\right] V_{CE}$$

$$= -\left[\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C}$$

We can draw a straight line on the graph of I_C versus V_{CE} which is having slope -1/Rc.To determine the two points on the line we assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$

a) When $V_{CE} = V_{CC}$; $I_C = 0$ and we get a point A
b) When $V_{CE} = 0$; $I_C = V_{CC}/R_C$ and we get a point B

The figure below shows the output characteristic curves for the transistor in CE mode. The DC load line is drawn on the output characteristic curves. **Load line -** To draw load line, we have to find saturation current and the cutoff voltage.

Saturation point - The point at which the load line intersects the characteristic curve near the collector current axis is referred to as the **saturation point**. At this point of time, the current through the transistor is maximum and the voltage across collector is minimum for a given value of load. So, saturation current for the fixed bias circuit, **Ic (sat) =Vcc/Rc** .

Cutoff point -The point where the load line intersects the cutoff region of the collector curves is referred as the cutoff point (i.e. end of load line). At this point, collector current is approximately zero and emitter is grounded for fixed bias circuit. so, **Vce (cut) = Vc = Vcc**

Operating point - The **"Q point"** for a transistor amplifier circuit is the point along its operating region in a "quiescent ", where no input signal gets amplified.

The figure below shows the output characteristic curves for the transistor in CE mode with points A and B, and line drawn between them. The line drawn between points A and B is called d.c load line. The d.c word indicates that only d.c conditions are considered, i.e input signal is assumed to be zero.

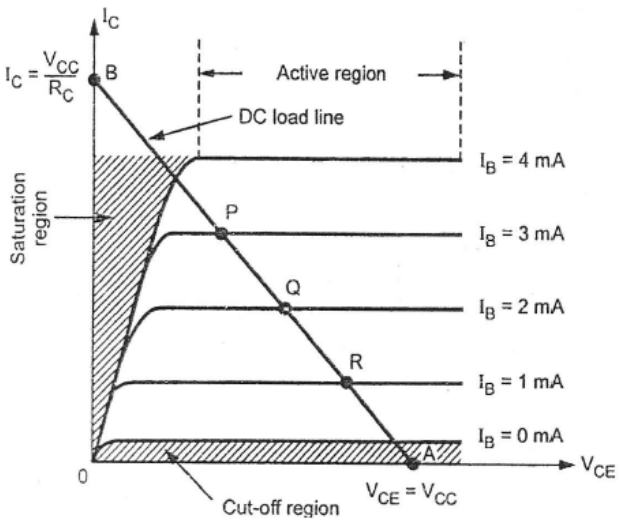


Fig 1.3

The d.c load line is a plot of I_C versus V_{CE}. For a given value of Rc and a given value of Vcc. So, it represents all collector current levels and corresponding collector emitter voltages that can exist in the circuit. Knowing any one of Ic, I_B, or V_{CE} , it is easy to determine the other two from the load line. The slope of the d.c load line depends on the value of R_C. It is the negative and equal to reciprocal of the R_C.

Applying KVL to the base circuit, we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The intersection of curves of different values I_B of with d.c load line gives different operating points. For different values of I_B, we have different intersection points such as P, Q and R.

Selection of operating point

The operating point can be selected at different positions on the d.c load line, near saturation region, near cut-off region or at the centre, i.e in the active region. The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the d.c. load line to prevent any possible distortion in the amplified output signal.

Case 1

Biasing circuit is designed to fix a Q point at point P which is very near to the saturation region. It results collector current is clipped at the positive half cycle. i.e. distortion is present at the output. Therefore, point P is not a suitable operating point.

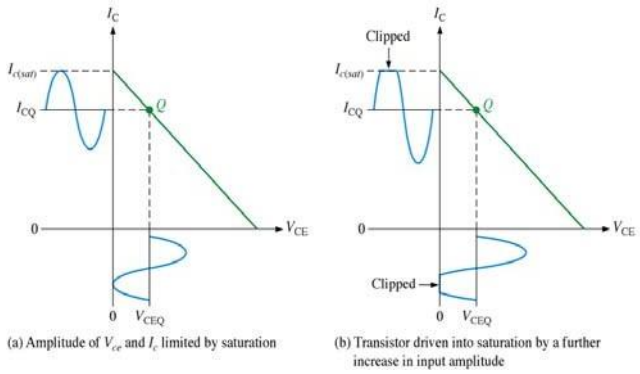


Fig 1.4

Case 2

Biasing circuit is designed to fix a Q point at point R as shown in Fig. Point R is very near to the cut-off region. Here, the collector current is clipped at the negative half cycle. So, point R is also not a suitable operating point.

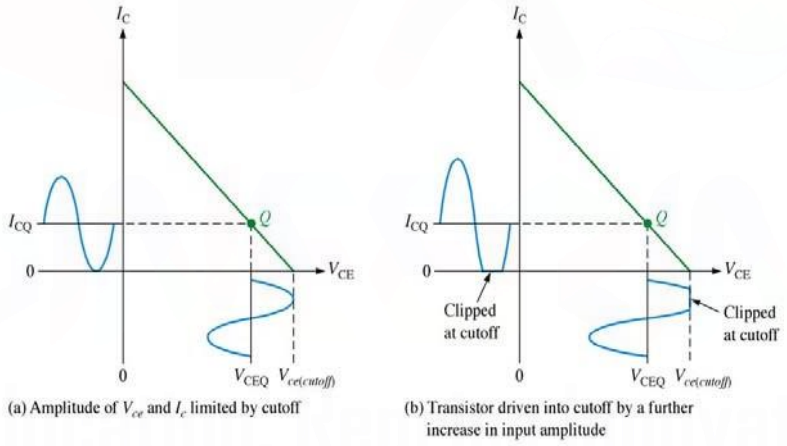


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Fig 1.5

Case 3

Biasing circuit is designed to fix a Q point at point Q as shown in Fig.. The output signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.

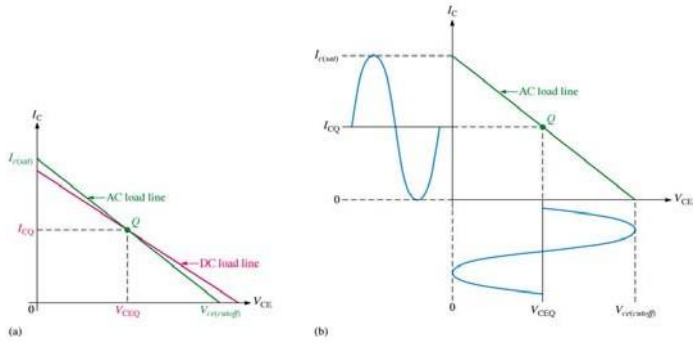


Fig 1.6

DC Load Line (Example)

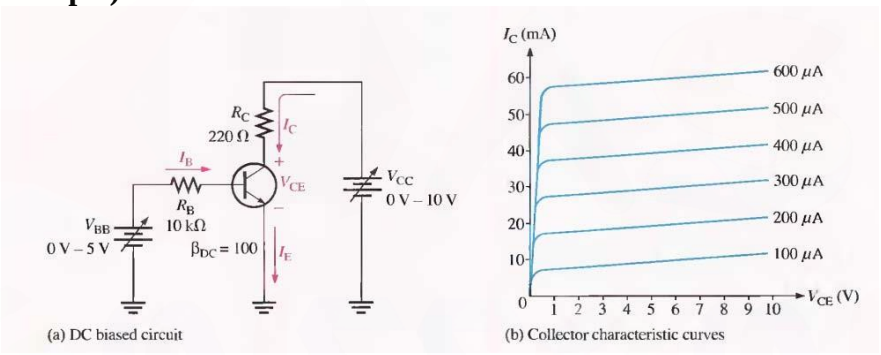


Fig 1.7

The figure 1.7 shows the biasing of transistor in common emitter configuration.

In Figure 1.8, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 A, as shown in Figure 1.8(a), Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$V_{CE} = V_{CC}$ - IcRc = 10 V - (20 mA) (220 Ω) = 10 V - 4.4 V = 5.6 V

This Q-point is shown on the graph of Figure 1.3(b) as Q1.

Next, as shown in Figure 1.8(b), V_{BB} is increased to produce an I_B of 300 μA and an Ic of 30mA.

V_{CE} = 10 V - (30 mA) (220 Ω) = 10V – 6.6 V = 3.4 V

The Q-point for this condition is indicated by Q2 on the graph.

Finally. as in Figure 1.8 (c), V_{BB} is increased to give an I_B of 400 μA and an Ic of 40 mA.

V_{CE} = 10 V - (40 mA) (220 Ω) = 10 V - 8.8 V = 1.2 V

Q3 is the corresponding Q-point on the graph.

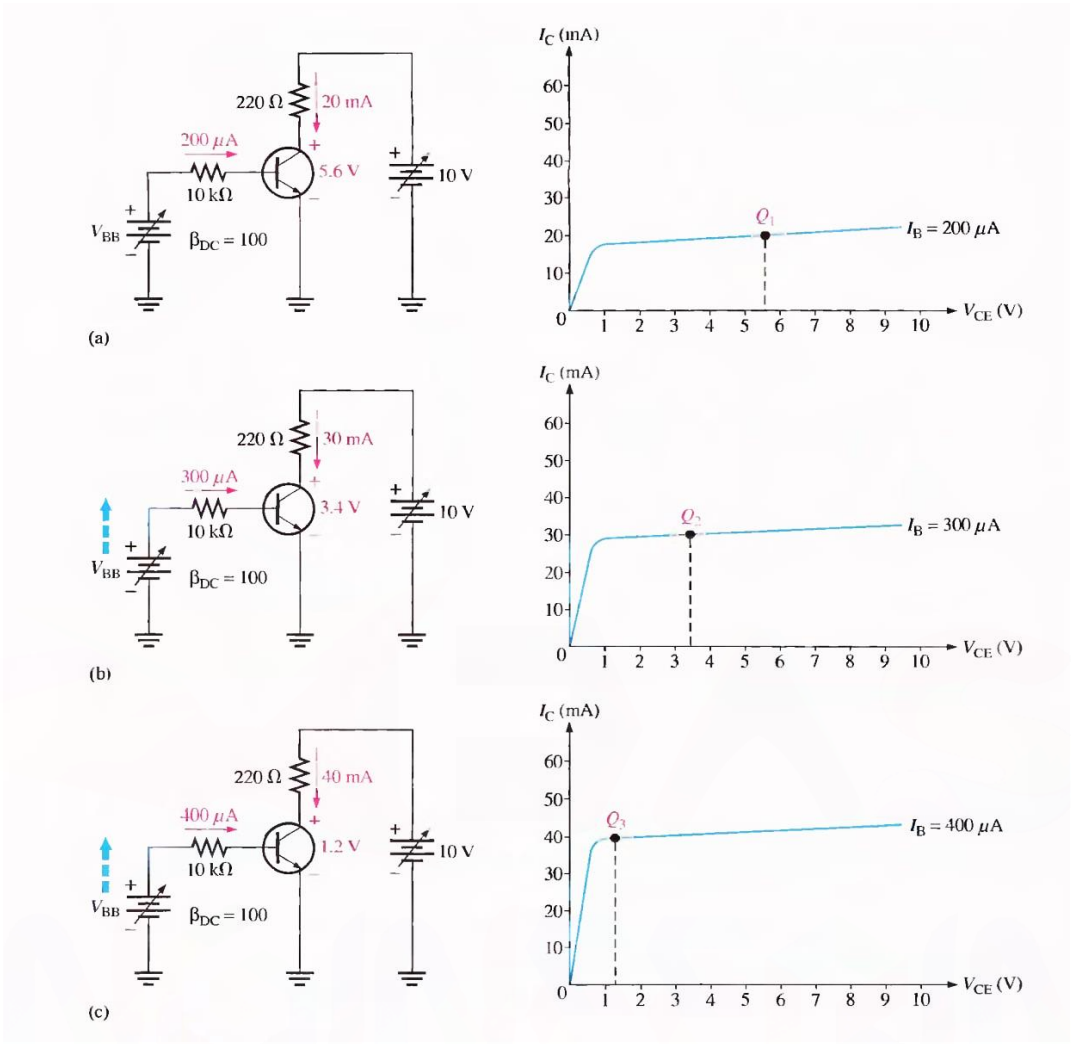


Figure 1.8

Notice that when I_B increases, Ic increases and V_{CE} decreases. When I_B decreases, Ic decreases and V_{CE} increases. As V_{BB} is adjusted up or down, the dc operating point of the transistor moves along a sloping straight line, called the DC load line, connecting each separate Q-point.

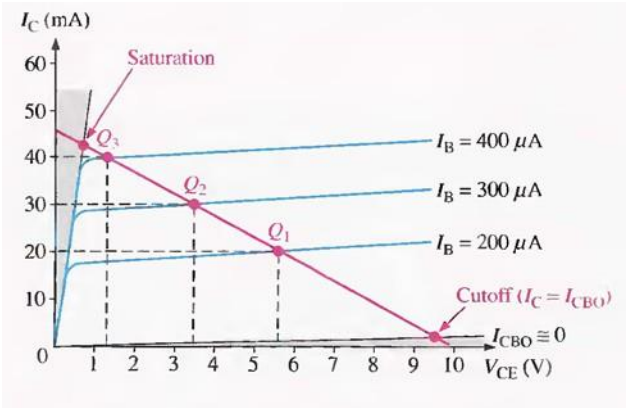


Figure 1.9

At any point along the line, values of I_B, Ic, and V_{CE} can be picked off the graph, as shown in Figure1.9.

The dc load line intersects the V_{CE} axis at 10 V. The point where $V_{CE} = V_{CC}$. This is the transistor cutoff point because I_B and I_C are zero (ideally). Actually, there is a small leakage current, I_{CBO} , at cutoff as indicated, and therefore V_{CE} is slightly less than 10 V but normally this can be neglected.

The dc load line intersects the I_C axis at 45.5 mA ideally. This is the transistor saturation point because I_C is maximum at the point where $V_{CE} = 0$ V and $I_C = V_{CC} / R_C$.

Actually, there is a small voltage ($V_{CE\ (sat)}$) across the transistor, and $I_{C(sat)}$ is slightly less than 45.5 mA, as indicated in Figure 1.4. Note that Kirchhoff's voltage law applied around the collector loop gives,

$$V_{CC} - I_C R_C - V_{CE} = 0.$$

These results in a straight line equation for the load line of the form $y = mx + b$ as follow:

$$I_C = - (1/R_C)\, V_{CE} + V_{CC} / R_C$$

Where, $- (1/R_C)$ is the slope and V_{CC} / R_C is the y-axis intercept point.

Variation of quiescent point due to h_{FE} variation within manufacturers tolerance

It is clear that the biasing circuit should be designed to fix the operating point or Q point at the center of the active region. But only fixing of the operating point is not sufficient. While designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region (i.e. into cut-off or saturation region). Designing the biasing circuit to stabilize the Q point is known as bias stability.

Two important factors are to be considered while designing the biasing circuits which are responsible for, shifting the operating point.

I. Temperature

1) Ico: The flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions". We know that the minority carriers are temperature dependent. They increase with the temperature. The increase in the minority carriers increases the leakage current I_{CE0},

$$I_{CEO} = (1 + \beta)\, I_{CBO}$$

Specifically, I_{CB0} doubles for every 10°C rise in temperature. Increase in I_{CE0} in turn increases the collector current

$$I_C = \beta I_B + I_{CEO}$$

The increase in I_C further raises the temperature at the collector junction and the same cycle repeats. This excessive increase in I_C shifts the operating point into the saturation region, changing the operating condition set by biasing circuit.

As the power dissipated within a transistor is predominantly the Power dissipated at its collector base junction, the power dissipation is given as

$$P_D = V_C I_C$$

The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increases

the collector current. The process is cumulative. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called 'Thermal runaway' of the transistor. For any transistor, maximum Power dissipation is always a fixed value. That is known as maximum power dissipation rating of a transistor. This value is specified by the manufacturer in data sheet. If this limit is crossed, the device will fail.

2) V_{BE} : Base to emitter voltage V_{BE} changes with temperature at the rate of 2.5mV/°C Base current, I_B depends upon V_{BE} .As base current I_B depends on $V_{BE,}$ and Ic depends on I_B, Ic depends on V_{BE}. Therefore collector current Ic. Change with temperature due to change in V_{BE}. The change in collector current change the operating point.

3)βdc: βdc of the transistor is also temperature dependent. As βdc varies, Ic also varies, since Ic = βI_B. The change in collector current change the operating point.
Therefore, to avoid thermal instability, the biasing circuit should be designed to provide a degree of temperature stability i.e. even though there are temperature changes, the changes in the transistor parameters (V_{CE} , I_{CQ} , $P_D$max)should be very less so that the operating point shifting is minimum in the middle of the active region.

II) Transistor current gain h_{FE}/β

Eventhough there is tremendous advancement in semiconductor technology, there are changes in the transistor parameters among different units of the same type, same number. This means if we take two transistor units of same fire (i.e. same number, construction, parameter specified etc.) and use them in the circuit, there is change in the β value in actual practice. The biasing circuit is designed according to the required **β** value. But due to change in β from unit to unit, the operating point may shift
Figure shows the common emitter output characteristics for two transistors of the same type. The dashed characteristics are for a transistor whose p is much larger than that of the transistor represented by the solid curves.
So for stabilizing the operating point the factors discussed so far should be considered while designing the biasing circuit.

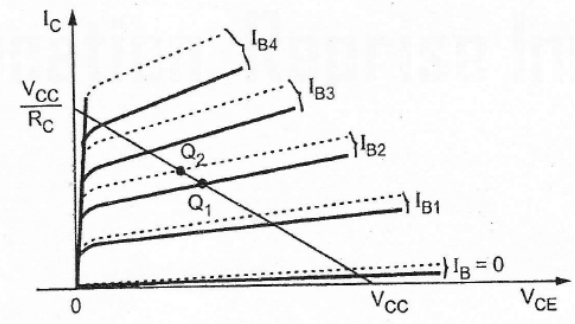


Figure: Common emitter output characteristics

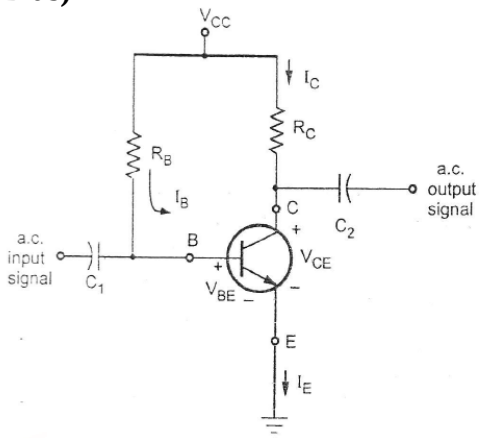
1.4 BIASING METHODS

The common biasing circuits used in the bipolar transistor amplifiers are

1. Fixed bias
2. Collector-to-base bias
3. Fixed bias with emitter resistor

4. Voltage divider bias
5. Emitter bias

1.5 Fixed Bias (Base Resistor Bias)



The Figure shows the fixed bias circuit. It is the simplest d.c. bias configuration. For the d.c. analysis we can replace capacitor with an open circuit because the reactance of a capacitor for d.c. is

$$X_C = 1 / 2\pi fC = 1 / 2\pi(0)C = \infty.$$

In the base circuit,
Apply KVL, we get

$$V_{CC} = I_B R_B + V_{BE}$$

Therefore,

$$I_B = (V_{CC} - V_{BE})/R_B$$

For a given transistor, V_{BE} does not vary significantly during use. As V_{CC} is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

In the Collector circuit
Apply KVL, we get

$$V_{CC} = I_C R_C + V_{CE}$$

Therefore,

$$V_{CE} = V_{CC} - I_C R_C$$

The common-emitter current gain of a transistor is an important parameter in circuit design, and is specified on the data sheet for a particular transistor. It is denoted as β.

$$I_C = \beta I_B$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$V_{CE} = V_C - V_E$$

$$V_{BE} = V_B - V_E$$

In this circuit $V_E = 0$

$$V_{BE} = V_B$$

$$V_{CE} = V_C$$

Stability factor S for Fixed bias circuit

Stability Factor S

$$I_B \cong \frac{V_{CC}}{R_B}$$

When I_B changes by ∂I_B, V_{CC} and V_{BE} are unaffected.

$\therefore \frac{\partial I_B}{\partial I_C} = 0$ $\because I_C$ is not present in the equation.

Substituting this value in equation , we get,

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} = \frac{1+\beta}{1-0}$$

$\therefore$ $S = 1 + \beta$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

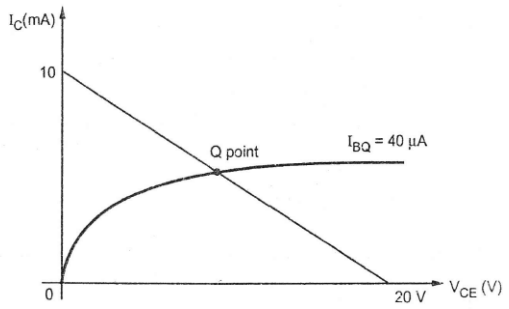
- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gain of the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.
- For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway. In particular, the stability factor, which is a measure of the change in collector current with changes in reverse saturation current, is approximately β+1. To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.

Usage:

Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch. However, one application of fixed bias is to achieve crude automatic gain control in the transistor by feeding the base resistor from a DC signal derived from the AC output of a later stage.

Problems

1. Design the fixed bias circuit from the load line given in the figure.



Solution : From the load line we have,

$$V_{CC} = 20 \text{ V}$$

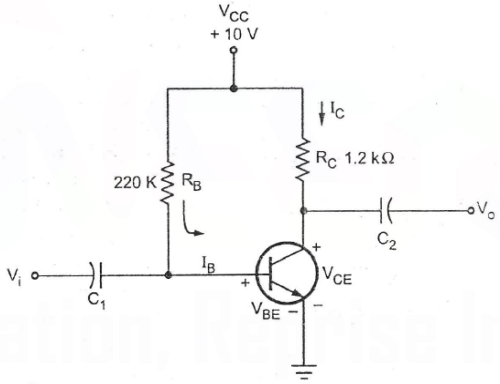
$$\frac{V_{CC}}{R_C} = 10 \times 10^{-3} \qquad \therefore \quad R_C = \frac{20}{10 \times 10^{-3}} = 2 \text{ K}$$

We have, $$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 - 0.7 \text{ V}}{40 \times 10^{-6}}$$

$$= \mathbf{482.5\ k\Omega}$$

2. For the circuit shown in figure. Calculate I_B,I_C,V_{CE},V_B,V_C and V_{BC}. Assume V_{BE}= 0.7V and β=50.



Solution : $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{220 \times 10^3} = \mathbf{42.27\ \mu A}$$

$$I_C = \beta I_B = 50 \times 42.27 \times 10^{-6} = \mathbf{2.1135\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^3$$

$$= \mathbf{7.4638\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V}$$

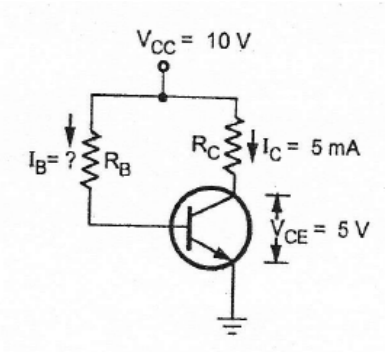
$$V_C = V_{CE} = \mathbf{7.4638\ V}$$

$$V_{BC} = V_B - V_C = 0.7 - 7.4638 = \mathbf{-6.7638}$$

The negative voltage V_{BC} **indicates that base-collector junction is reverse biased.**

3. Design a fixed biased circuit using a silicon transistor having β value of 100. Vcc is 10 V

and dc bias conditions are to be V_{CE} = 5 V and I_C = 5 mA,



Solution

Applying KVL to collector circuit,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$\therefore R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10 - 5}{5\,mA} = 1\ K$$

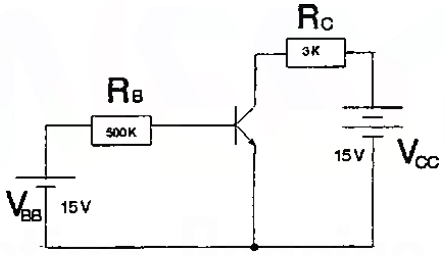
$$I_B = \frac{I_C}{\beta} = \frac{5\,mA}{100} = 50\ \mu A$$

Applying KVL to base circuit,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{50\,\mu A} = 186\ k\Omega$$

4. Calculate the operating point (Q-point)



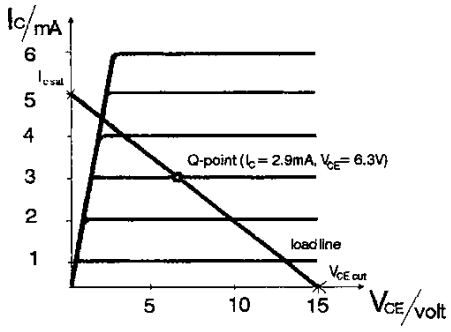
Base biased CE connection

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{14.3V}{500K\Omega} = 29\mu A$$

$I_C = \beta_{dc} * I_B = 100 * 29\mu A = 2.9$ mA

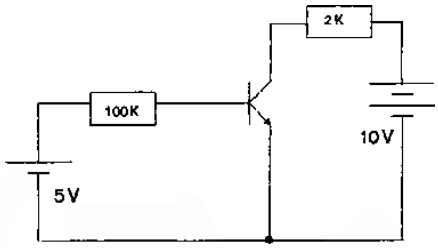
$V_{CE} = V_{CC} - (I_C * R_C) = 15V - (2.9\ mA * 3K\Omega) = 6.3V$

By plotting I_C (2.9 mA) and V_{CE} (6.3V), we get the operation point ----> Q-point (quiescent point).



Collector curve with load line and Q – point

5. Draw the load line and Q-point.



base biased CE connection, β=50

Solution:

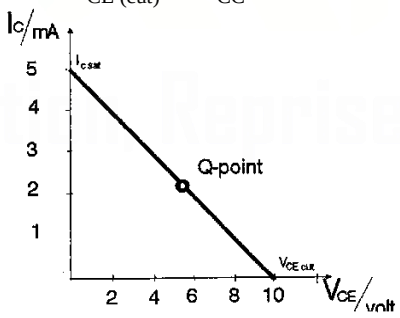
$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = 0.043mA$$

$I_C = I_B * \beta = 2.15$ mA

$V_{CE} = V_{CC} - (R_C * I_C) = 5.7V$

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = 5mA$$

$V_{CE\ (cut)} = V_{CC} = 3.0V$



1.6 Requirements of a biasing circuit

1. Emitter base junction must be forward biased and collector base junction must be reverse biased. That means the transistor should be operated in the middle of the active region or Q point should be fixed at the centre of the active region.
2. Circuit design should provide a degree of temperature stability.
3. Q point should be made independent of the transistor parameters such as β.

To maintain the Q point stable by keeping I_C and V_{CE} constant so that the transistor will always work in active region, the following techniques are normally used,

1. Stabilization technique
2. Compensation technique

1.7 Method of stabilizing the Q point

Stabilization technique:

It refers to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C relatively constant with variations in I_{CO}, β and V_{BE}.

Compensation technique:

It refers to the use of temperature sensitive devices such as diodes, transistors, thermistors which provide compensating voltage and current to maintain Q point stable.

1.8 Stability Factors

It is defined as the degree of change in operating point due to variation in temperature. There are three variables which are temperature dependent. Three stability factors are defined as follows,

i) $$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}} \quad \text{or} \quad S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}}$$

ii) $$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}} \quad \text{or} \quad S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$$

iii) $$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$$

Stability factor S:

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$

or $$I_C = \beta I_B + (1+\beta) I_{CBO}$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C. equation becomes,

$$\partial I_C = \beta \partial I_B + (1+\beta) \partial I_{CBO}$$

$$\therefore \quad 1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad \frac{\partial I_{CBO}}{\partial I_C} = \frac{1 - \beta (\partial I_B / \partial I_C)}{1+\beta}$$

$$S = \frac{\partial I_C}{\partial I_{CBO}}$$

$$S = \frac{(1+\beta)}{1-\beta(\partial I_B/\partial I_C)}$$

The above equation can be considered as a standard equation for the derivation of stability factors of other biasing circuits.

Stability factor S':

$$S' = \frac{\partial I_C}{\partial V_{BE}}\bigg|_{I_{CO},\beta \text{ constant}}$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

Stability factor S":

$$S'' = \frac{\partial I_C}{\partial \beta}\bigg|_{V_{BE}, I_{CO} \text{ constant}}$$

From equation (1.7.7) we have $I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta + 1) I_{CBO}$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CBO} = I_B + I_{CBO} = \frac{I_C}{\beta}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \quad \text{Since } I_B = \frac{I_C}{\beta} \text{ and } I_B >> I_{CBO}$$

Relation between S and S":

We know that $S = 1+\beta$ and $S'' = I_C/\beta$

Multiplying numerator and denominator by $(1+\beta)$,

$$S'' = \frac{I_C(1+\beta)}{\beta(1+\beta)}$$

$$S'' = I_C \frac{S}{\beta(1+\beta)}$$

1.9 Collector to Base Bias

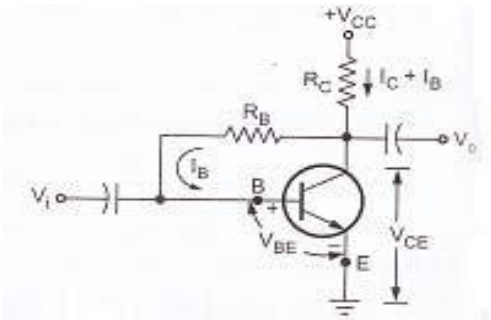


Fig. D.C. bias with voltage feedback

Figure shows the dc bias with voltage feedback. It is also called as collector to base bias circuit. It is an improvement over fixed bias method. In this, biasing resistor is connected between collector and base of the transistor to provide feedback path.

Circuit analysis:

Base circuit:

Consider the base circuit and applying voltage law then we get,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$= (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \qquad \because \beta >> 1$$

Only the difference between the equation for I_B and that obtained for fixed bias configuration is βR_C, so the feedback path results in a reflection of the resistance R_C to the input circuit.

Collector circuit:

Applying KVL to the collector circuit,

$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - (I_C + I_B) R_C$

If there is a change in β due to piece to piece variation between transistors or if there is a change in β and I_{CO} due to the change in temperature. So collector current tends to increase. As a result, voltage drop across R_C increases. Due to reduction in V_{CE}, I_B reduces. The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

In this circuit, R_B appears directly across input and output. A part of output is feedback to the input. And increase in collector current decreases the base current. So negative feedback exists in the circuit. It is also called as voltage feedback bias circuit.

1.10 Modified collector to base bias circuit:

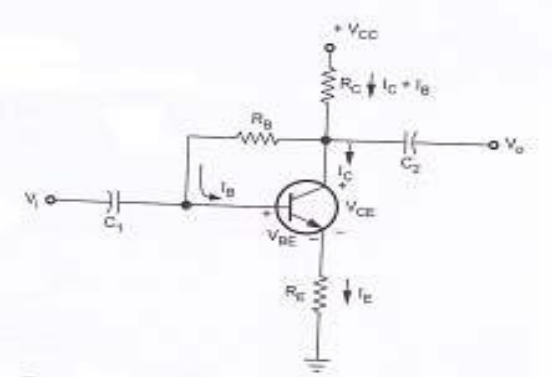


Fig. Modified d.c. bias with voltage feedback

To improve the level of stability, emitter resistance is connected in this circuit.

Base circuit:

Applying KVL to base circuit,

$V_{CC} – (I_C + I_B) RC – I_B R_B – V_{BE} – I_E R_E = 0$

$$I_B = \frac{V_{CC} – V_{BE}}{R_B + (1+\beta)(R_C + R_E)}$$

$$I_B = \frac{V_{CC} – V_{BE}}{R_B + \beta (R_C + R_E)}$$

Only difference between the equation for I_B and that obtained for the fixed bias configuration is the term $\beta (R_C + R_E)$.So feedback path results in a reflection of the resistance R_C back to the input circuit.

In general,

$$I_B = \frac{V'}{R_B + \beta R'}$$

Where $V' = V_{CC} - V_{BE}$

$R' = 0$ for fixed bias

$R' = R_E$ for emitter bias

$R' = R_C$ for collector to base bias

$R' = R_C + R_E$ for collector to base bias with R_E

Collector circuit:

Applying KVL to collector circuit,

$V_{CC} – (I_C+I_B) RC – V_{CE} – I_E R_E = 0$

$V_{CE} = V_{CC} – I_E (R_C+R_E)$

Stability factor S for collector to base bias circuit:

$V_{CC} = I_C RC – I_{B(}R_B+R_C) + V_{BE}$

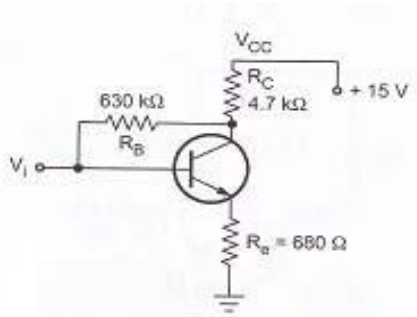
When I_{CBO}, I_B and I_C changes with no effect on VCC and V_{BE}, the equation becomes,

$$S = \frac{1+\beta}{1+\beta\,(R_C/(R_C+R_B))}$$

Collector to base bias circuit is having lesser stability factor than for fixed bias circuit. So this circuit provides better stability than fixed bias circuit.

Problem 1:

Locate the operating point of the given circuit with V_{CC} = 15V, h_{fe} = 200.



Solution:

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C+R_E)}$$

$$= \frac{15-0.7}{630*10^3 + (1+200)(4.7*10^3+680)}$$

$I_{CQ} = \beta\, I_{BQ} = 200*8.356*10^{-6}$

$= 1.6712\text{mA}$

$I_{EQ} = I_{CQ} + I_{BQ} = 1.6712*10^{-3} + 8.356*10^{-6}$

$= 1.68\text{mA}$

$V_{CEQ} = V_{CC} - I_E\,(R_C+R_E)$

$= 15-1.68*10^{-3}\,(4.7*10^3 + 680)$

$= 5.96\text{V}$

1.11 Voltage divider bias circuit:

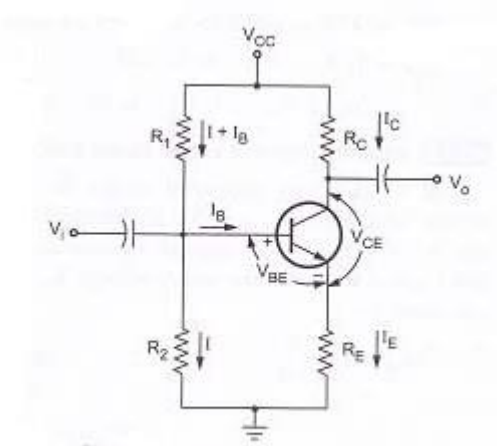


Fig. Voltage divider bias circuit

Figure shows the voltage divider bias circuit. In this, biasing is provided by three resistors R_1, R2 and R_E. The resistors R_1 & R_2 act as a potential divider giving a fixed voltage to base. If collector current increases due to change in temperature or change in β, emitter current I_E also increases and voltage drop across R_E increases thus reducing the voltage difference between base and emitter. Due to reduction in base emitter voltage, base current and collector current reduces. So we can say that negative feedback exists in emitter bias circuit. This reduction in collector current compensates for the original change in I_C.

Circuit analysis:

Base circuit:

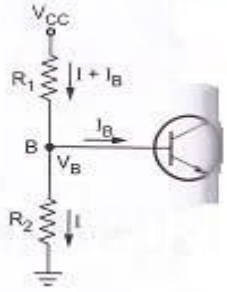


Fig. Base circuit

Let us consider the base circuit as shown in above figure. Voltage across R_2 is base voltage V_B. Applying voltage divider rule to find V_B,

$$V_B = \frac{R_2 (I)}{* V_{CC}R_1 (I+I_B) + R_2 (I)}$$

$$= \frac{R2}{R_1+R_2} * V_{CC} \quad \text{with } I>>I_B$$

Collector circuit:

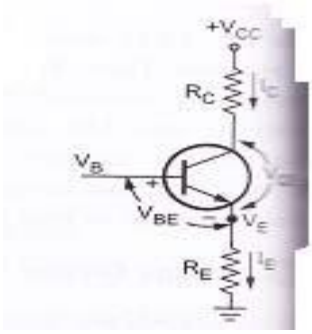


Fig. Divider biased

Let us consider the collector circuit as shown in above figure. Voltage across R_E can be obtained as,

$V_E = I_E R_E = V_B - V_{BE}$

$I_E = \frac{V_B - V_{BE}}{R_E}$

Apply KVL to collector circuit,

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

Simplified circuit of voltage divider bias:

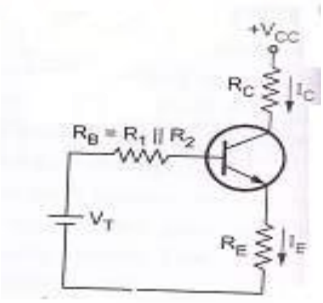


Fig. Thevenin's equivalent circuit for voltage divider bias

From above figure, R_1 and R_2 are replaced by R_B and V_T.

Where R_B is the parallel combination of R=1 and R_2

V_T is the thevenin's voltage

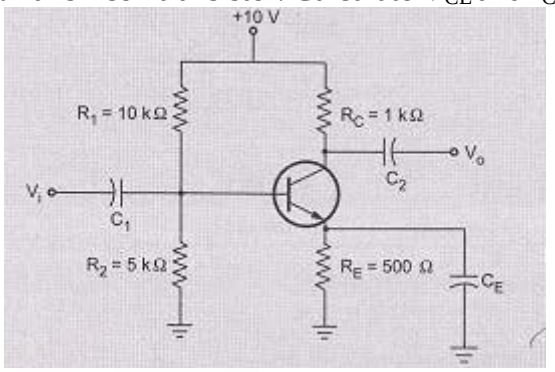
$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Apply KVL,

$$V_T = I_B R_B + V_{BE} + I_E R_E$$
$$V_T = V_{BE} + (R_B + R_E) I_B + I_C R_E$$
$$V_{BE} = V_T - (R_B + R_E) I_B - I_C R_E$$

Problem 1:

For the given circuit β=100 for silicon transistor. Calculate V_{CE} and I_C.



Solution:

$$V_T \cong \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = \mathbf{3.33\ V}$$

$$R_B = \frac{10 \times 5}{10 + 5} = 3.33\ \text{k}\Omega$$

Applying KVL to the base circuit we get,

$$V_T - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E} = \frac{3.33 - 0.7}{3.33 \times 10^3 + (101) 500} = \mathbf{48.86\ \mu A}$$

$$I_C = \beta I_B = 100 \times 48.86\ \mu\text{A} = \mathbf{4.886\ mA}$$

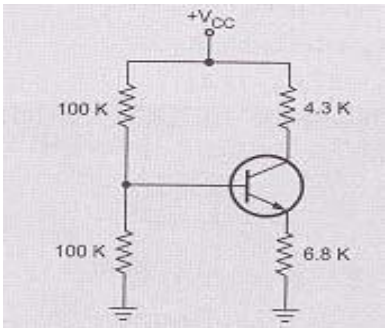
$$I_E = \mathbf{4.935\ mA}$$

Applying KVL to collector circuit we have,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$
$$= 10 - 4.886 \times 1 - 4.935 \times 0.5 = \mathbf{2.6465\ V}$$

Problem 2:

For the given figure find Q point with V_{CC} = 15V, V_{BE} = 0.7V and β = 100.



Solution:

$$V_T \cong \frac{R_2}{R_1 + R_2} V_{CC} = \frac{100 \times 10^3}{100 \times 10^3 + 100 \times 10^3} \times 15 = \mathbf{7.5\ V}$$

$$R_B = 100\ K \,||\, 100\ K = \mathbf{50\ K}$$

Applying KVL to the base circuit we get,

$$V_T - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$\therefore \quad I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E} = \frac{7.5 - 0.7}{50 \times 10^3 + (101)\, 6.8 \times 10^3} = \mathbf{9.23\ \mu A}$$

$$I_C = \beta I_B = 100 \times 9.23\ \mu A = \mathbf{0.923\ mA}$$

$$I_E = \mathbf{0.932\ mA}$$

Applying KVL to collector circuit we have,

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 15 - 0.923 \times 4.3 - 0.932 \times 6.8 = \mathbf{4.6935\ V}$$

Therefore, Q point : I_{CQ} = **0.923 mA** and V_{CEQ} = **4.6935 V.**

Stability factor for voltage divider bias:
Stability factor S:

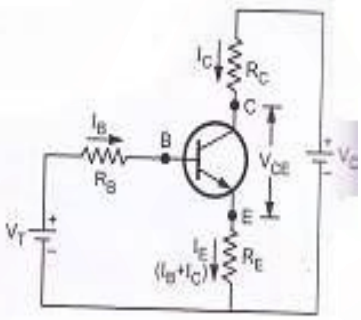


Fig. Thevenin's equivalent circuit for voltage divider bias

For determining stability factor S for voltage divider bias, consider the equivalent circuit. Thevenin's voltage is given by,

$$V_T = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

R_1, R2 are replaced by R_B which is the parallel combination of R_1 and R_2.

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Apply KVL to base circuit,

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating with respect to I_C and considering V_{BE} to be independent of I_C,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\frac{\partial I_B}{\partial I_C}(R_E + R_B) = -R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B}$$

Stability factor S is given by,

$$S = \frac{1+\beta}{1-\beta(\partial I_B/\partial I_C)}$$

From above equation, the following points are observed.

1. The ratio R_B/R_E controls value of stability factor S. If $R_B/R_E << 1$ then it is reduced to $S = (1+\beta).\ 1/\ (1+\beta) = 1$

Practically R_B/R_E not equal to zero. But to have better stability factor S , we have to keep ratio R_B/R_E as small as possible.

2. To keep R_B/R_E small, it is necessary to keep R_B small. Due to small value of R_1 and R_2, potential divider circuit will draw more current from V_{CC} reducing the life of the battery. Another important aspect is that reducing R_B will reduce input impedance of the circuit, since R_B comes in parallel with the input. This reduction of input impedance in amplifier circuit is not desirable and hence R_B cannot be made very small.

3. Emitter resistance R_E is another parameter, it is used to decrease the ratio R_B/R_E. Drop across R_C will reduce. This shifts the operating point Q which is not desirable and hence there is limit for increasing R_E.

While designing voltage divider bias circuit, the following conditions are to be satisfied,

S – Small

R_B - Reasonably small

R_E - Not very large

4. If ratio R_B/R_E is fixed, S increases with β. So stability decreases with increasing β.

5. Stability factor S is essentially independent of β for small value of S.

Substituting the differentiation value of I_B/I_C,

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

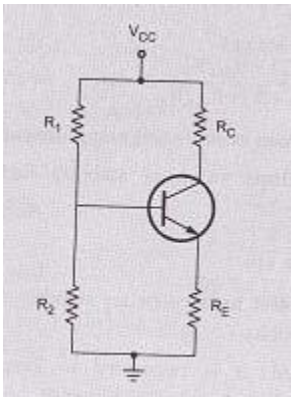
Dividing each term by R_E,

$$S = \frac{(1+\beta)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

$$S = (1+\beta)\frac{1+R_B/R_E}{(1+\beta)+R_B/R_E}$$

Problem 1:

For the given circuit, V_{CC} = 20V, R_C = 2KΩ, β = 50, V_{BE} = 0.2V, R_1 = 100KΩ, R_E = 100Ω. Calculate I_B, V_{CE}, I_C and stability factor S.



Solution:

R_2 is not given. So assume $R_2 = 10K\Omega$

$$V_T = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{20 \times 10}{100+10} = 1.818 \text{ V}$$

$$R_B = \frac{R_1 * R_2}{R_1 + R_2} = 9.09K\Omega$$

$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta)R_E} = 114\mu A$$

$I_C = \beta I_B = 5.7Ma$

$V_{CE} = V_{CC} - I_C R_C - (1+\beta) I_B R_E$

$= 8V$

$$S = \frac{1+\beta}{1+\beta\,(R_E / (R_E + R_B))}$$

$S = 33$

1.12 Compensation technique:

It refers to the use of temperature sensitive devices such as diodes, transistors, thermistors which provide compensating voltage and current to maintain Q point stable.

1.12.1 Diode Compensation Techniques

Compensation for V_{BE}:

a) Diode in Emitter Circuit

Diagram shows the voltage divider bias with bias compensation technique.Here, separate supply V_{DD} is used to keep diode in forward If biased condition. If the diode used in the circuit is of same material and type as the transistor, the voltage across the diode will have the same temperature coefficient as the base to emitter voltage V_{BE} . So when V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D and

$\partial V_D \approx \partial V_{BE}$, the changes tend to cancel each other.

Apply*g KVL to the base circuit of Fig. ,we have

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E - V_D$$
$$= I_B (R_B + R_E) + I_C R_E + V_{BE} - V_D$$

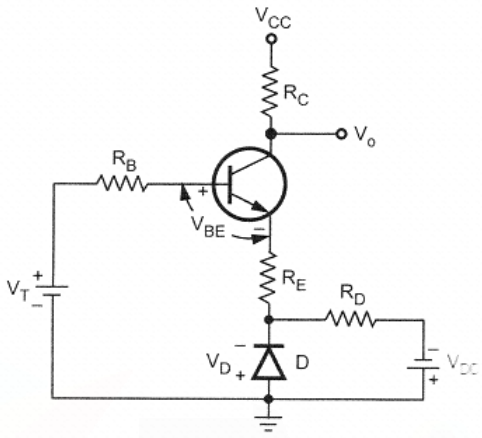


Figure: Stabilization by means of voltage divider bias and diode Compensation Technique

Considering leakage current we have,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$\therefore \quad I_B = \frac{I_C}{\beta} + \frac{(1+\beta) I_{CO}}{\beta}$$

Substituting the value of I_B in equation 1.9.1 we have

$$V_T = \left[\frac{I_C}{\beta} + \frac{(1+\beta) I_{CO}}{\beta}\right] (R_B + R_E) + I_C R_E + V_{BE} - V_D$$

$$= \frac{I_C}{\beta} (R_B + R_E) + \frac{\beta I_C R_E}{\beta} + \frac{(1+\beta) I_{CO} (R_B + R_E)}{\beta} + V_{BE} - V_D$$

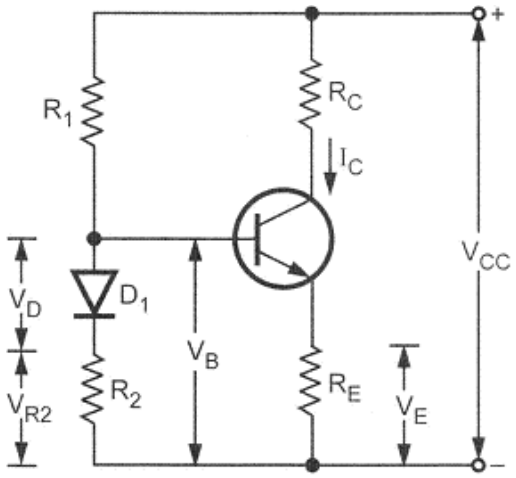
$$= \frac{I_C}{\beta} [R_B + (1+\beta) I_E] + \frac{(R_B + R_E)(1+\beta) I_{CO}}{\beta} + V_{BE} - V_D$$

$$\therefore \quad \frac{I_C}{\beta} [R_B + (1+\beta) R_E] = V_T - V_{BE} + V_D + \frac{(R_B + R_E)(1+\beta) I_{CO}}{\beta}$$

$$\therefore \quad I_C = \frac{\beta [V_T - (V_{BE} - V_D)] + (R_B + R_E)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

As V_D tracks V_{BE} with respect to temperature it is clear that I_C will be insensitive to variations in $V_{BE.}$

Diode in voltage divider circuit



Diode compensation in voltage divider bias circuit

- Diode is connected in series with resistance R_2 in the voltage divider circuit and it is forward biased condition.
  For voltage divider bias,

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{V_E}{R_E}$$

$$I_C \approx \frac{V_B - V_{BE}}{R_E} \qquad \because I_C \approx I_E$$

When V_{BE} changes with temperature, I_C also changes

- To cancel the changes in I_C, one diode is used in the circuit for compensation
- The voltage at the base V_B is give as

$$V_B = V_{R2} + V_D$$

Substituting this value in equation I_C, we get,

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

V_{BE} changes by ∂V_{BE}

V_D changes by ∂V_D and $\partial V_D \approx \partial V_{BE}$,

The changes cancel each other , so the collector current is given as

$$I_C \approx \frac{V_{R2}}{R_E}$$

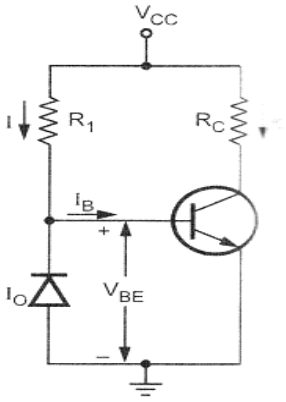
The changes in $V_{BE.}$ Due to temperature are compensated by changes in the diode voltage which keeps I_C stable at Q point.

Compensation for I_{CO}

* In germanium transistor changes in I_{CO} with temperature plays an important role collector current stability

* The diode is kept at reverse bias condition ,so only leakage current flows

* I_o increases then I_{CO} also increases



Diode compensation for a germanium transistor

$$I = \frac{V_{CC} - V_{BE}}{R_1}$$

and $I = I_B + I_O \quad \therefore I_B = I - I_O$

For germanium transistor $V_{BE} = 0.2$ V, which is very small and neglecting change in V_{BE} with temperature we can write,

$$I \cong \frac{V_{CC}}{R_1} \cong \text{constant}$$

We know, $I_C = \beta I_B + (1+\beta) I_{CO}$

Substituting value of I_B in above equation we get,

$$I_C = \beta I - \beta I_O - (1-\beta) I_{CO}$$

if $\beta >> 1$ we get,

$$I_C = \beta I - \beta I_O + \beta I_{CO}$$

Now if $I_O = I_{CO}$ we get,

$$I_C = \beta I$$

As I is constant , I_C also remains constant. We can say that changes by I_{CO} with temperature are compensated by diode and collector current remains constant

1.12.2 Thermistor Compensation

Thermistor Compensation

This method of transistor compensation uses temperature sensitive resistive elements, thermistors than diodes or transistors. It has a negative temperatur coefficient, its resistance decreases exponentiallt with increasing temperature as shown fig.

slope of this curve = $\frac{\partial R_T}{\partial T}$

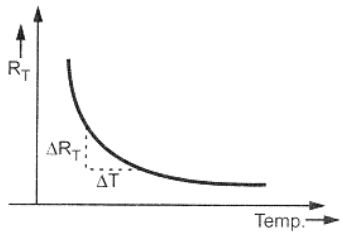


Fig. Temperature Vs R_T resistance of thermistor

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor

With increase of temperature ,R_T decreases. Hence the voltage drop across it also decreases. That is V_{BE} decreases which reduces I_B . this will offset the increased collector current with temperature.

$I_C = \beta I_B + (1+\beta) I_{CO}$

The equation shows if there is increase in I_{CO} and decrease in I_B keeps I_C almost constant.

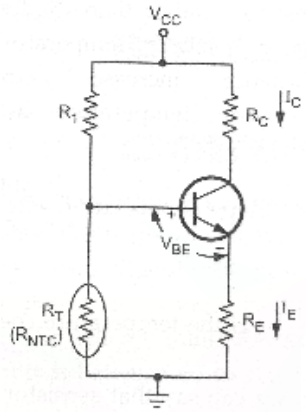


Fig.(a) Thermistor compensation technique

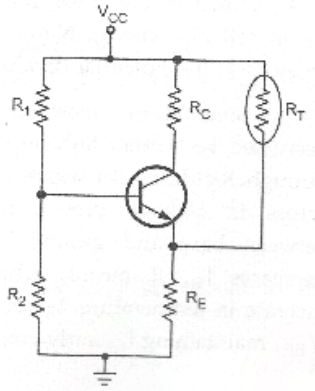


Fig. (b) Thermistor compensation technique

Fig (b) shows another thermistor compensation technique . Here, thermistor is connected between emitter and Vcc to minimize the increase in collector current due to changes in ICO, VBE, or beta with temperature .I_C increases with temperature and R_T decreases with increase in temperature. Therefore, current flowing through RE increases, which increases the voltage drop across it. E - B junction is forward biased. But due to increase in voltage drop across R_E, emitter is made more positive, which reduces the forward bias voltage V_{BE}. Hence, bias current reduces.

I_C is given by,

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

As Ico increases with temperature, I_B decreases and hence. IC remains constant

Sensistor Compensation technique

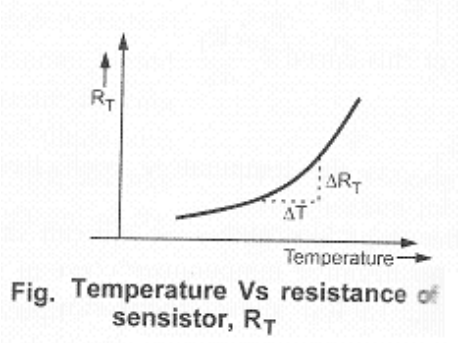


Fig. Temperature Vs resistance of sensistor, R_T

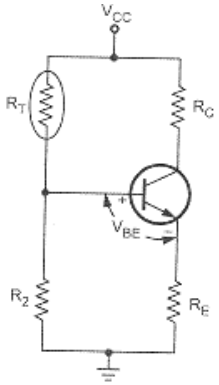


Fig. Sensistor compensation technique

This method of transistor compensation uses temperature sensitive resistive element, sensistors rather than diodes or transistors. It has a positive temperature coefficient, its resistance increases exponentially with increasing temperature as shown in the Fig

Slope of this curve = $\frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor and the slope is positive So we can say that sensistor has positive temperature coefficient of resistance (PTC).

Fig. shows sensistor compensation R_1 is replaced by sensistor R_T in self bias circuit. Now, R_T and R_2 resistors of the potential divider. As temperature increases, RT increases which decreases the current flowing through it. Hence current through R2 decreases which reduces the voltages drop across it. Voltage drop across R2 is the voltage between base and ground. So V_{BE} reduces which decreases 16. It means, when I_{CBO} increases with increase in temperature, I_B reduces due to reduction in V_{BE}, maintaining I_C fairly constant.

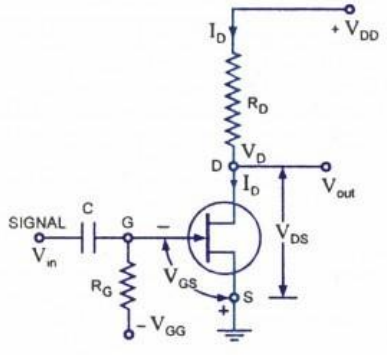
1.13 FET Biasing

- The Parameters of FET is temperature dependent .When temperature increases drain resistance also increases, thus reducing the drain current.
- Unlike BJTs, thermal runaway does not occur with FETs
- However, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple fixed-gate bias voltage.
- Different biasing circuits of FET are

1) Fixed bias circuits
2) Self bias circuits
3) Voltage bias circuits

Fixed bias circuits

DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D . For a JFET drain current is limited by the saturation current I_{DS}. Since the FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.



Fixed Biasing Circuit For JFET

Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor

R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ *i.e.* 0 volt.

Calculate V_{GS}

For DC analysis I_G =0., applying KVL to the input circuits

$V_{GS+} V_{GG=0}$

$V_{GS=} - V_{GG}$

As V_{GS} is a fixed dc supply, hence the name fixed bias circuit

Calculate I_{DQ}

$I_{DQ=} I_{Dss(1-} V_{GS/} V_{Gp)}^{2}$

Calculate V_{DS}

This current I_{DQ} then causes a voltage drop across the drain resistor R_D and is given as

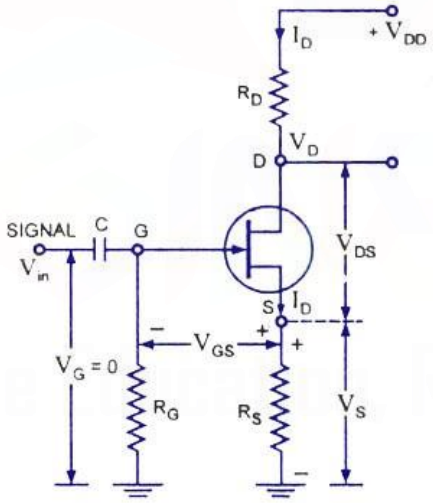
$V_{DSQ} = V_{DD} - I_D R_D$

Disadvantage

The fixed bias circuit of FET requires two power supplies.

Self-Bias circuits

Self-Bias circuits is the most common method for biasing a JFET. Self-bias circuit for N-channel JFET is shown in figure



Self-Bias Circuit For N-Channel JFET

- The gate source junction of JFET must be always in reverse biased condition .No gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and, therefore,$v_G = i_G R_G = 0$
- With a drain current I_D the voltage at the S is $V_s = I_D R_s$

1)The gate-source voltage is then

$V_{GS} = V_G - V_s = 0 - I_D R_S = - I_D R_S$

So voltage drop across resistance R_s provides the biasing voltage V_{Gg} and no external source is required for biasing and this is the reason that it is called self-biasing.

2)Calculate I_{DQ}

$I_{D=} I_{DSS}(1- V_{GS/} V_P)^2$

Substituting the value of V_{GS}

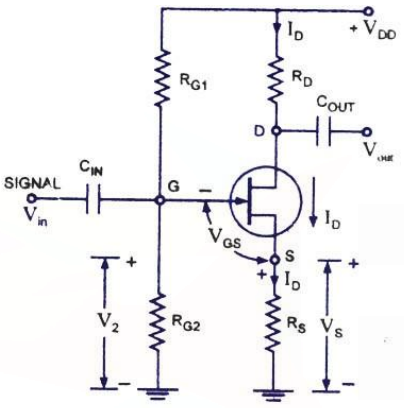
$I_{D=} I_{DSS} (1+I_D R_S / V_P)^2$

3)The operating point (that is zero signal I_D and V_{DS}) can easily be determined from equation given below :

$V_{DS} = V_{DD} – I_D (R_D + R_S)$

Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance. Any increase in voltage drop across R_S, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

Voltage -Divider Bias circuits



Potential-Divider Bias Circuit For N-Channel JFET

The resistors R_{Gl} and R_{G2} form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{Gl} from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued R_S.

The coupling capacitors are assumed to be open circuit for DC analysis

1) The gate is reverse biased so that $I_G = 0$ and gate voltage
   $V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$
2) Applying KVL to the input circuit we get
   $V_{GS} = V_G – V_S = V_G - I_D R_S$
3) $I_{DQ}= I_{DSS}(1- V_{GS}/ V_P)^2$
4) $V_{DS} = V_{DD} – I_D (R_D + R_S)$

   The operating point of a JFET amplifier using the Voltage -Divider Bias is determined by

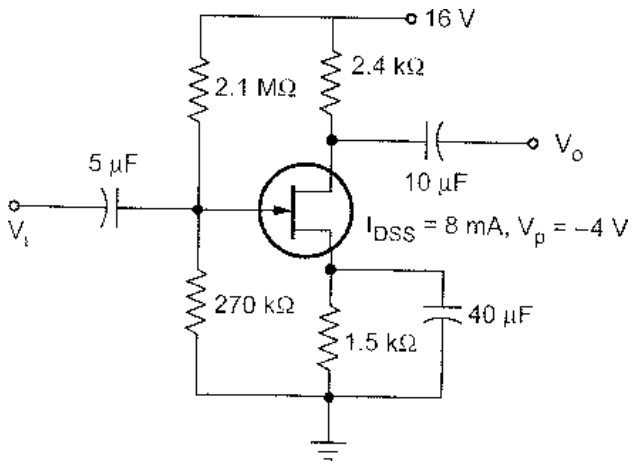
   $I_{DQ}= I_{DSS}(1- V_{GS}/ V_P)^2$

   $V_{DSQ} = V_{DD} – I_D (R_D + R_S)$

   $V_{GSQ} = V_G – I_D R_S$

Example Problems

1)Determine $I_{DQ,}$ $V_{GSQ,}$ $V_{D,}$ $V_{S,}$ $V_{DS,}$ and V_{DG}



Solution

Calculate V_G

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{16 \times 270\,K}{2.1\,M + 270\,K} = \mathbf{1.823\ V}$$

Obtain expression for V_{GS}

$$V_{GS} = 1.823 - I_D R_S = 1.823 - 1.5 \times 10^3\, I_D$$

Calculate I_D

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8 \times 10^{-3}\left(1 - \frac{(1.823 - I_D \times 1.5 \times 10^3)}{-4}\right)^2$$

$$= 8 \times 10^{-3}(1 - [(-0.456 + 375\, I_D)])^2 = 8 \times 10^{-3}(1.456 - 375\, I_D)^2$$

$$= 8 \times 10^{-3}\left(2.12 - 1092\, I_D + 140625\, I_D^2\right)$$

$$I_D = 0.01696 - 8.736\, I_D + 1125\, I_D^2$$

$$\therefore \quad 1125\, I_D^2 - 9.736 I_D + 0.01696 = 0$$

Solving quadratic equation using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we get,

$$= \frac{-(-9.736) \pm \sqrt{(-9.736)^2 - 4 \times 1125 \times 0.01696}}{2 \times 1125} = \frac{9.736 \pm 4.2976}{2 \times 1125}$$

$$= \textbf{6.237 mA} \quad \text{or} \quad \textbf{2.417 mA}$$

If we calculate value of V_{DS} taking $I_D = 6.237$ mA we get,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - 6.237 \times 10^{-3}(2.4\,K + 1.5\,K) = \textbf{– 8.3243 V}$$

Practically, the value of V_{DS} must be positive, hence

I_D = 6.237 mA is invalid.

$\therefore$ I_D = **2.417 mA**

Step 4 : Calculate V_{DS}, V_{GS}, V_S, V_D and V_{DG}.

$\therefore$ $V_{DS} = V_{DD} - I_D(R_D + R_S) = 16 - 2.417 \times 10^{-3}(2.4\,K + 1.5\,K) =$ **6.5737 V**

$V_{GS} = 1.823 - I_D R_S = 1.823 - (2.417 \times 10^{-3} \times 1.5 \times 10^3) =$ **– 1.8025 V**

$V_S = I_D R_S = 2.417 \times 10^{-3} \times 1.5 \times 10^3 =$ **3.6255 V**

$V_D = V_{DD} - I_D R_D = 16 - (2.417 \times 10^{-3} \times 2.4 \times 10^3) =$ **10.2 V**

$V_{DG} = V_D - V_G = 10.2 - 1.823 =$ **8.377 V**

Example 2. *For the circuit shown in Fig. 2. the FET has $V_p = 4$ V, $I_{DSS} = 4$ mA*
Calculate i) I_{DSQ} ii) V_{GSQ} iii) V_{DSQ}

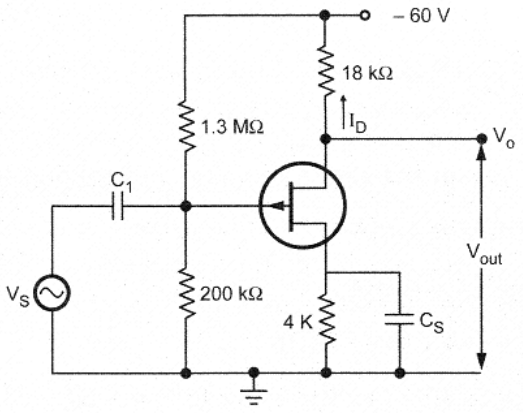


Fig. 2.

Simplified circuit for d.c. analysis is shown in Fig. 2.2.

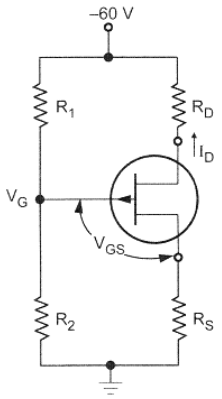


Fig. 2.2

1 : Calculate V_G

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{200 \times 10^3 \times (-60)}{1.3 \times 10^6 + 200 \times 10^3} = \mathbf{-8\ V}$$

2 : Obtain expression for V_{GS}

Applying KVL to input circuit we get,

$$V_G - V_{GS} + I_D R_S = 0$$

$$\therefore \quad V_{GS} = V_G + I_D R_S$$

$$V_{GS} = V_G + I_D R_S = \mathbf{-8 + I_D R_S}$$

Step 3 : Calculate I_D

We have, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in the above equation and solving for I_D we get,

$$I_D = 2.25 \text{ mA or } 4 \text{ mA}$$

We calculate V_{DS} using $I_D = 4$ mA,

$$V_{DS} = V_{DD} - (-I_D (R_S + R_D))$$

$$= -60 + 4 \times 10^{-3} (4 \times 10^3 + 18 \times 10^3) = -60 + 88 = \mathbf{28\ V}$$

Practically, value of V_{DS} for p-channel FET should be negative, hence $I_D = 4$ mA is invalid.

$$\therefore \quad I_D = \mathbf{2.25\ mA}$$

Step 4 : Calculate V_{DS} and V_{GS} .

Now calculating V_{DS} taking I_D = 2.25 mA,

$$V_{DS} = -60-(-2.25\times10^{-3}\,(4\times10^{3}+18\times10^{3})) = -60-49.5 = \mathbf{-10.5\ V}$$

$$V_{GS} = -8+I_D R_S = -8+2.25\times10^{-3}\,(4\times10^{3}) = -8+9 = \mathbf{1\ V}$$

Example for Practice:

For circuit shown in Fig. , Calculate I_D , V_{GS} , V_G, V_{DS} and $\mathbf{V_S}$

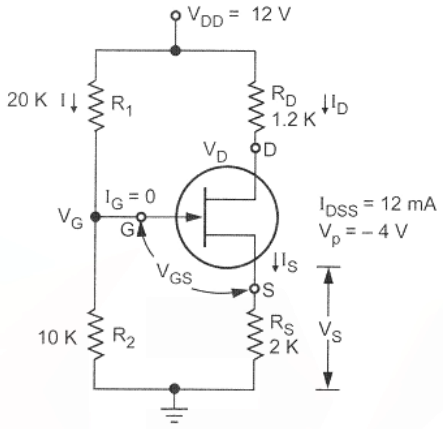


Fig. 2.2.9

[V_G = 4 V, I_D = 3 mA, V_{DS} = 2.4 V, V_{GS} = – 2 V and V_S = 6

*Example 4

Example *Calculate the value of feedback resistor (R_s) required to self bias . . JFET with I_{DSS} = 40 mA, V_P = – 10 and V_{GSQ} = – 5 V.*

Solution :

Step 1 : Calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left[1-\frac{V_{GSQ}}{V_P}\right]^2 = 40\times10^{-3}\left[1-\frac{(-5)}{(-10)}\right]^2 = \mathbf{10\ mA}$$

Step 2 : Calculate R_S

For self bias circuit : $V_{GSQ} = -I_{DQ}R_S$

$$\therefore \quad R_s = \frac{-V_{GSQ}}{I_{DQ}} = \frac{-(-5)}{10\ \text{mA}} = \mathbf{500\ \Omega}$$

Example Problem

Calculate the value of feedback resistor (R_s) required to self bias JFET with I_{DSS} = 40 mA, V_P = – 10 and V_{GSQ} = – 5 V.

Solution :

Step 1 : Calculate I_{DQ}

$$I_{DQ} = I_{DSS}\left[1-\frac{V_{GSQ}}{V_P}\right]^2 = 40\times10^{-3}\left[1-\frac{(-5)}{(-10)}\right]^2 = \mathbf{10\ mA}$$

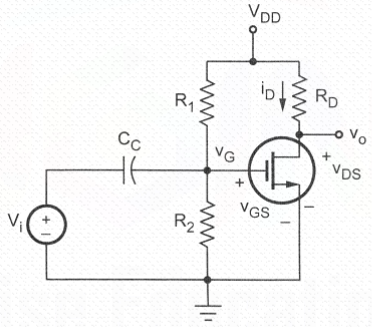
Step 2 : Calculate R_S

For self bias circuit : $V_{GSQ} = -I_{DQ}R_S$

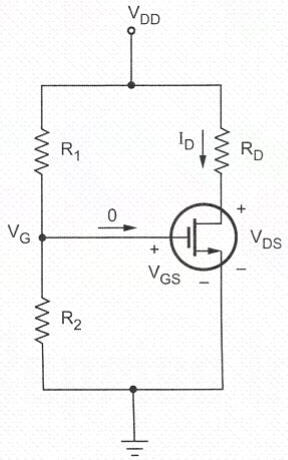
$$\therefore \quad R_s = \frac{-V_{GSQ}}{I_{DQ}} = \frac{-(-5)}{10\ mA} = \mathbf{500\ \Omega}$$

1.14 Biasing of MOSFET

*N-channel enhancement mode MOSFET circuit shows the source terminal at ground potential and is common to both the input and output sides of the circuit.
*The coupling capacitor acts as an open circuit to d.c. but it allows the signal voltage to be coupled to the gate of the MOSFET.



An nMOS common-source circuit



d.c. equivalent circuit

As $I_g = 0$ in V_G is given as,

$$V_G = V_{GS} = \left(\frac{R_2}{R_1+R_2}\right)V_{DD}$$

Assume $V_G > V_T$, MOSFET is biased in the saturation region, the drain current is,

$$I_D = K(V_{GS} - V_T)^2$$

Applying KVL to drain circuit we have,

$$V_{DS} = V_{DD} - I_D R_D$$

If $V_{DS} > V_{DS(sat)} = V_{GS} - V_T$, then the MOSFET is biased in the saturation region,
If $V_{DS} < V_{DS(sat)}$, then the MOSFET is
Biased in the nonsaturation region, and the drain current is given by, I_D

Example problem-1

RD=40

For the circuit shown in Fig. , assume that $R_1 = 30\ k\Omega$, $R_2 = 10\ k\Omega$, $k\Omega$, $V_{DD} = 10\ V$, $V_T = 1V$, $V_{GS} = 2\ V$ and $K = 0.1\ mA/V^2$. Find I_D and V_{DS}.

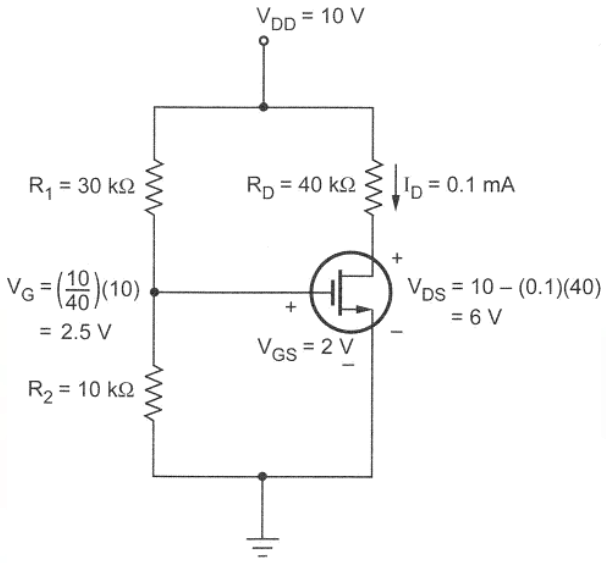


Fig.

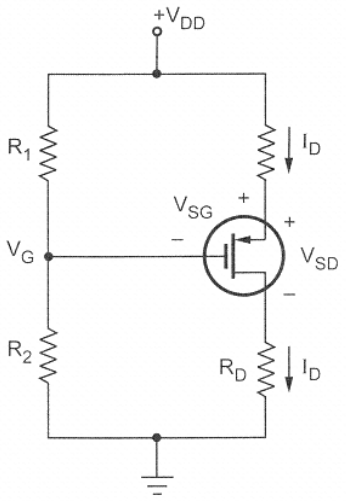
$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{10}{10+30}\right)(10) = 2.5\ V$$

Assuming the MOSFET is biased in the saturation region, the drain current is,

shows a common-source circuit with a p-channel **enhancement-mode** MOSFET.

$$V_{DS} = V_{DD} - I_D R_D = 10 - (0.1)\,(40) = 6\ V$$

Validity of assumption : Because $V_{DS} = 6\ V > V_{DS(sat)} = V_{GS} - V_T = 2 - 1 = 1\ V$, the MOSFET is indeed biased in the saturation region and our calculations are valid.



A pMOS common-source circuit

Here, the source is tied to $+V_{DD}$, which become signal ground in the a.c. equivalent circuit. Thus it is also a common-source circuit.

The d.c. analysis for this circuit is essentially the same as for the n-channel MOSFET circuit. The gate voltage is given by,

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

and the source-to-gate voltage is given by,

$$V_{SG} = V_{DD} - V_G$$

Assuming that $V_{GS} < V_T$, or $V_{SG} > |V_T|$, and that the device is biased in the saturation region, the drain current is given by,

$$I_D = K(V_{SG} + V_T)^2$$

and the source-to-drain voltage is,

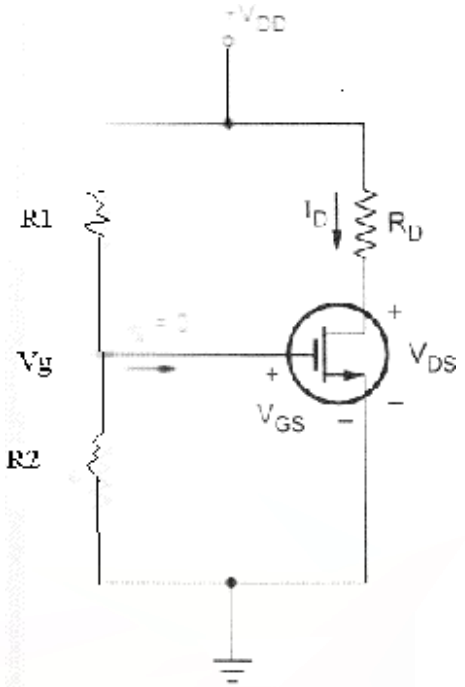
$$V_{SD} = V_{DD} - I_D R_D$$

If $V_{SD} > V_{SD(sat)} = V_{SG} + V_T$, then the MOSFET is indeed biased in the saturation region, as we have assumed. However, if $V_{SD} < V_{SD(sat)}$, the MOSFET is biased in the nonsaturation region.

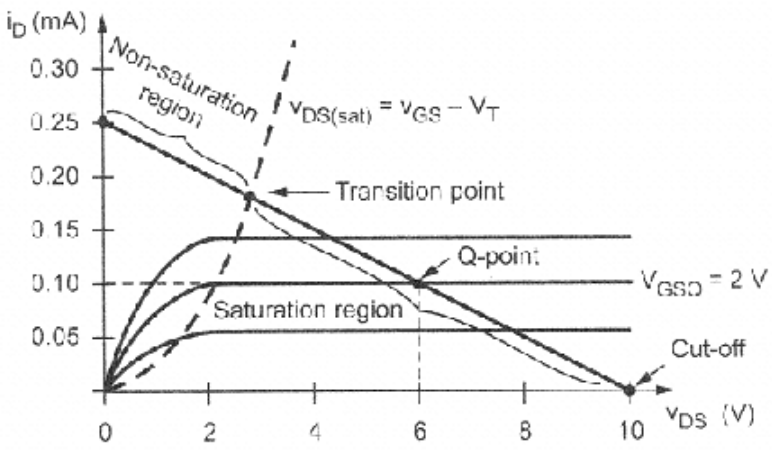
Load Line and Modes of Operation

The load line gives a graphical picture showing the region in whichthe MOSFET is biased. Consider the common-source circuit shown in Fig. (a).

Writing Kirchhoff's voltage law around the drain-source loop results $V_{Ds} = V_{DD} - I_{DRD}$, which is the load line equation. It shows a linear relationship between the drain current and drain-to-source voltage. Fig. (b) shows the $V_{DS(sat)}$ characteristic for the MOSFET



(a) Common source circuit



(b) Transistor characteristics, $V_{DS(sat)}$ curve, loadline and Q-point for the nMOS common-source circuit shown in Fig.

The load line is given by

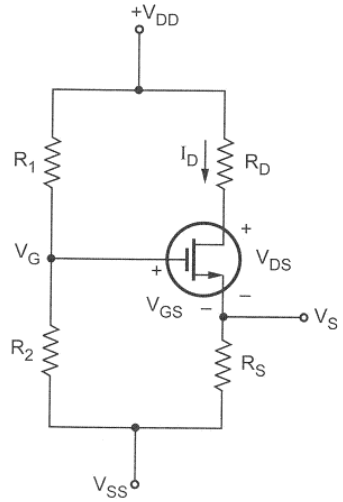
$$V_{DS} = V_{DD} - I_D R_D = 10 - I_D(40)$$

$$I_D = \frac{10}{40} - \frac{V_{DS}}{40} \text{ (mA)}$$

The two end points of the load line are determine in the usual manner. If the drain current = 0, then V_{DS}= 10 v; if V_{DS} = 0, then drain current = 10/40 = 0.25 mA. The Q-point of the MOSFET is given by the d.c. drain current (I_D) and drain-to-source voltage (V_{DS}) and it is always on the load line, as shown in the Fig. b).

If the gate-to-source voltage is less than V1, the drain current is zero and the MOSFET is in cut-off. As the gate-to-source voltage becomes just greater than the threshold voltage, the MOSFET turns ON and is biased in the saturation region. As V_{GS} increases, the Q-point moves up the load line. The transition point is the boundary between the saturation and non-saturation regions. It is the point where, $V_{DS} = V_{DS(sat)} = V_{GS} - V_T$. As V_{GS} increases further, the MOSFET operates in un saturation region.

Common Source circuit for EMOSFET with source resistor



nMOS common-source circuit with source resistor

Voltage Divider Bias

As

$$I_G = 0\ A$$

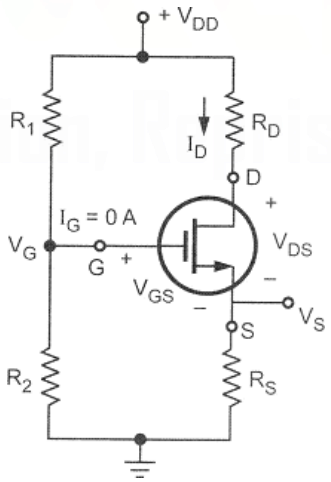
$$V_G = \frac{R_2\, V_{DD}}{R_1 + R_2}$$

Applying KVL to input circuit we get,

$$V_{GS} - V_S = 0$$

$$V_{GS} = V_G - I_S R_S = V_G - I_D R_D \quad \because I_D = I_S$$

$$V_{GS} = V_G - I_D R_S$$



Applying KVL to output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D - I_S R_S = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S)$$

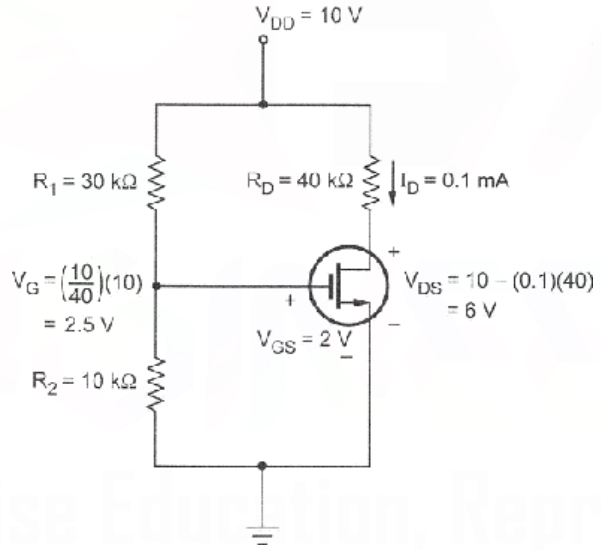
Because $I_D = I_S$

Biasing Circuit for D MOSFET

Biasing circuits for depletion type MOSFET are quite similar to the circuits used for JFET biasing. The primary difference between the two is the fact that depletion type MOSFETs also permit operating points with positive value of V6s for n-channel and negative values of V6s for p-channel MOSFET. To have positive value of V_{GS} for n-channel and negative value of V6s for p-channel self bias circuit is unsuitable.

Example problem-1

For the circuit shown in Fig. assume that $R_1 = 30\,k\Omega$, $R_2 = 10\ k\Omega$, $R_D = 40\ k\Omega$, $V_{DD} = 10\ V$, $V_T = 1V$, $V_{GS} = 2\ V$ and $K = 0.1\ mA/V^2$. Find I_D and V_{DS}.



$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{10}{10+30}\right)(10) = 2.5\ V$$

Assuming the MOSFET is biased in the saturation region, the drain current is,

$$I_D = K(V_{GS} - V_T)^2 = (0.1)\,(2-1)^2 = 0.1\,mA$$

and the drain-to-source voltage is,

$$V_{DS} = V_{DD} - I_D R_D = 10 - (0.1)\,(40) = 6\ V$$

Validity of assumption : Because $V_{DS} = 6\ V > V_{DS(sat)} = V_{GS} - V_T = 2 - 1 = 1\ V$, the MOSFET is indeed biased in the saturation region and our calculations are valid.

Fig. shows a common-source circuit with a p-channel enhancement mode MOSFET.

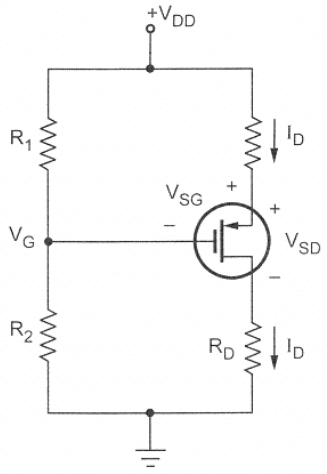


Fig. A pMOS common-source circuit

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

and the source-to-gate voltage is given by,

$$V_{SG} = V_{DD} - V_G$$

Assuming that $V_{GS} < V_T$, or $V_{SG} > |V_T|$, and that the device is biased in the saturation region, the drain current is given by,

$$I_D = K(V_{SG} + V_T)^2$$

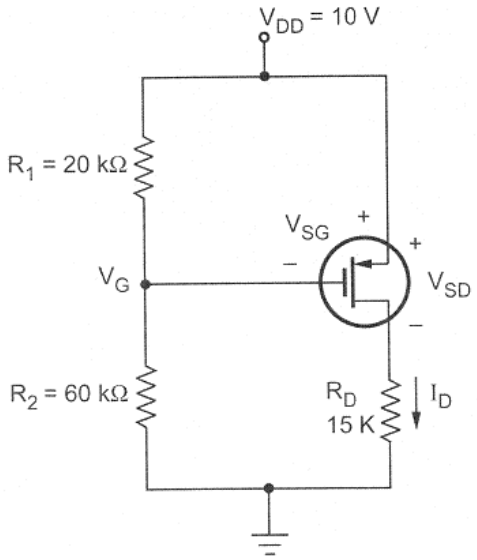
and the source-to-drain voltage is,

$$V_{SD} = V_{DD} - I_D R_D$$

If $V_{SD} > V_{SD(sat)} = V_{SG} + V_T$, then the MOSFET is indeed biased in the saturation region, as we have assumed. However, if $V_{SD} < V_{SD(sat)}$, the MOSFET is biased in the nonsaturation region.

Example – 2

Consider the circuit shown in Fig. Assume that, $R_1 = 20\ k\Omega$, $R_2 = 60\ k\Omega$, $V_{DD} = 10\ V$, $R_D = 15\ k\Omega$, $V_T = -0.8\,V$, *and* $K = 0.2\ mA/V^2$. *Find* I_D *and* V_{SD}.



From the circuit shown in Fig. 2.4.5 we have,

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{60}{20+60}\right)(10) = 7.5 \text{ V}$$

The source-to-gate voltage is therefore,

$$V_{SG} = V_{DD} - V_G = 10 - 7.5 = 2.5 \text{ V}$$

Assuming the MOSFET is biased in the saturation region, the drain current is,

$$I_D = K(V_{SG} + V_T)^2 = (0.2)\,(2.5 - 0.8)^2 = 0.578 \text{ mA}$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D = 10 - (0.578)\,(15) = 1.33 \text{ V}$$

Since $V_{SD} = 1.33$ V is not greater than $V_{SD(sat)} = V_{SG} + V_T = 2.5 - 0.8 = 1.7$ V, the p-channel MOSFET is not biased in the saturation region, as we initially assumed.

In the nonsaturation region, the drain current is given by,

$$I_D = K[2(V_{SG} + V_T)V_{SD} - V_{SD}^2]$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D$$

Combining these two equation, we obtain

$$I_D = K[2(V_{SG} + V_T)(V_{DD} - I_D R_D) - (V_{DD} - I_D R_D)^2]$$

For simplicity, we take resistance values in kΩ so we get value of I_D in mA.

$$I_D = (0.2)[2(2.5 - 0.8)(10 - I_D(15)) - (10 - I_D(15))^2]$$

$$I_D = (0.2)[3.4(10 - 15\, I_D) - (100 - 300\, I_D + 225\, I_D^2)]$$

$$= (0.2)[34 - 51\, I_D - 100 + 300 I_D - 225\, I_D^2]$$

$$I_D = (0.2)[-66 + 249\, I_D - 225\, I_D^2]$$

$$\therefore \quad 45\, I_D^2 - 48.8\, I_D + 13.2 = 0$$

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{48.8 \pm \sqrt{(-48.8)^2 - 4 \times 45 \times 13.2}}{2 \times 45}$$

$$= \frac{48.8 \pm 2.33238}{90}$$

$$= 0.568 \text{ mA} \quad \text{or } 0.5163 \text{ mA}$$

$$V_{SD} = V_{DD} - I_D R_D$$

$$= 10 - 0.568 \times 15 \quad \text{or} \quad 10 - 0.5163 \times 15$$

$$= 1.48 \text{ V} \quad \text{or} \quad 2.2555 \text{ V}$$

To bias MOSFET in non-saturation region $V_{SD} < V_{SD(sat)}$, the $V_{SD} = 1.48$ V satisfies this condition and hence $I_D = 0.568$ mA is valid. Thus,

$$I_D = \mathbf{0.568\ mA} \text{ and } V_{SD} = \mathbf{1.48\ V}$$

Example-3

Consider the circuit shown in Fig. Assume $V_T = 1$ V and $K = 0.1$ mA/V^2. Determine the transition parameters for the given circuit.

Solution : At the transition point,

$$V_{DS} = V_{DS(sat)} = V_{GS} - V_T = V_{DD} - I_D R_D$$

The drain current is still

$$I_D = K(V_{GS} - V_T)^2$$

Substituting expression of I_D in equation (1) we get,

$$V_{GS} = V_T = V_{DD} - K R_D (V_{GS} - V_T)^2$$

Rearranging this equation gives

$$K R_D (V_{GS} - V_T)^2 + (V_{GS} - V_T) - V_{DD} = 0$$

or $$(0.1)(40)(V_{GS} - V_T)^2 + (V_{GS} - V_T) - 10 = 0$$

$$4(V_{GS} - V_T)^2 + (V_{GS} - V_T) - 10 = 0$$

$$V_{GS} - V_T = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{-1 \pm \sqrt{1^2 - 4 \times 4 \times (-10)}}{2 \times 4} = \frac{-1 \pm 12.68857}{8}$$

$$= 1.461 \text{ V or } 1.711 \text{ V}$$

Taking the smaller value we have,

$$\therefore \quad V_{GS} - V_T = 1.461 \text{ V} = V_{DS}$$

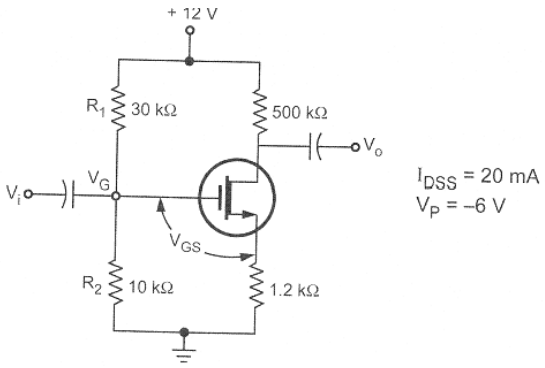
Therefore $V_{GS} = 2.461$ V

and $$I_D = (0.1) \times 10^{-3} (2.461 - 1)^2 = \mathbf{0.2134\ mA}$$

For $V_{GS} < 2.461$ V the MOSFET is biased in the saturation region and $V_{GS} > 2.461$ V, the MOSFET is biased in the nonsaturation region.

Example-4

For the circuit shown in Fig. calculate I_D , V_{DS} , V_G, and V_S.



Applying KVL to the input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - V_S$$

$$= 3 - I_S R_S \quad \because V_S = I_S R_S$$

$$= 3 - I_D R_S \quad \because I_D = I_S$$

We have, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{(3 - I_D R_S)}{V_p}\right)^2 = 20\times 10^{-3}\left(1 - \frac{(3 - I_D \times 1.2\times$$

$$= 20\times 10^{-3}\,(1 - [\,(-0.5) + 200\, I_D\,])^2 = 20\times 10^{-3}\,(1.5 -$$

$$= 20\times 10^{-3}(2.25 - 600\, I_D + 40000\, I_D^2)$$

$$\therefore \quad I_D = 0.045 - 12\, I_D + 800\, I_D^2$$

$$\therefore \quad 800\, I_D^2 - 13\, I_D + 0.045 = 0$$

Solving quadratic equation using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we get,

$$= \frac{-(-13) \pm \sqrt{(13)^2 - 4(800)(0.045)}}{2(800)}$$

$$= \frac{13 \pm \sqrt{169 - 144}}{1600} = \frac{13 \pm \sqrt{25}}{1600} = \frac{13 \pm 5}{1600} = 5 \text{ mA or } 11.25 \text{ mA}$$

If we calculate value of V_{DS} taking $I_D = 11.25$ mA we get,

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 12 - 11.25 \times 10^{-3} (500 + 1.2 \times 10^3)$$

$$= 12 - 19.125 = -7.125$$

Practically, the value of V_{DS} must be positive, hence $I_D = 11.25$ mA is invalid.

Now calculating value of V_{DS} taking $I_D = 5$ mA,

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 12 - 5 \times 10^{-3} (500 + 1.2 \times 10^3) = 12 - 8.5 = \mathbf{3.5\ V}$$

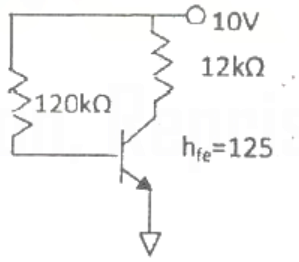
$$V_{GS} = 3 - I_D R_S = 3 - 5 \times 10^{-3} \times 1.2 \times 10^3 = 3 - 6 = \mathbf{-3\ V}$$

$$V_S = I_D R_S = 5 \times 10^{-3} \times 1.2 \times 10^3 = \mathbf{6\ V}$$

QUESTIONS

2 MARK

1. What is DC load line? Draw the DC load line of the circuit shown in fig.



2. Find the collector and base current of circuit diagram given in fig, having $h_{fe} = 100$, $V_{BE(on)} = 0.7V$

3. Why do we choose Q point at the center of the load line?
4. What is operating point?
5. Distinguish between dc and ac load line with suitable diagram.
6. Name the two techniques used in the stability of the q point .explain.
7. Define the stability factor.
8. Define three stability factors.
9. List out the different types of biasing.
10. What is the need for the biasing the transistor amplifier?
11. What is the requirements for biasing circuits?
12. Define the term biasing.
13. Draw the fixed bias single stage transistor circuit.
14. Derive the stability factor S for a fixed bias circuit.
15. What are the advantages of fixed bias circuit?
16. Draw a single stage self biased circuit using pnp transistor.
17. What are the factors against which an amplifier needs to be stabilized?
18. What is thermal runway? How it can be avoided.
19. Why the transistor is called a current controlled device?
20. Define current amplification factor?
21. What is the necessary of the coupling capacitor?
22. Draw the any two biasing circuit for a JFET.
23. Draw any one biasing circuit for depletion type MOSFET.
24. Draw the any two biasing circuit for an enhancement type MOSFET.
25. Explain how an FET is used as a voltage variable resistor.

16 MARK

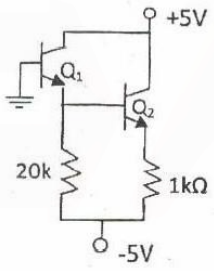
1. Explain the voltage divider bias method & derive an expression for stability factors.
2. Why biasing is necessary in BJT amplifier? Explain the concept of DC & AC load line with neat diagram.
3. How will you select the operating point, explain it using CE amplifier characteristics?
4. Explain the collector feedback bias amplifier & derive an expression for stability factors.
5. Explain the fixed bias method & derive an expression for stability factors.
6. Derive an expression for all stability factors & CE configuration S equation.
7. Explain about common source self- bias & voltage divider bias for FET.
8. Explain in details about biasing MOSFET.
9. Discuss the various types of bias compensation.
10. Explain constant current biasing used in JFET amplifier. *(May,06)*
11. Draw and explain voltage divider bias using FET and derive for its stability factors. Also mention its advantages. *(May,11)*
12. How is a JFET used as a voltage variable resistance? Explain. *(Nov,07) (May,07)*
13. Explain the bias circuit for enhancement MOSFET and explain its operation. *(Nov,14; Nov,13)*
14. With circuit diagram explain biasing of FET and MOSFET. *(Nov,07)*
15. Discuss the various techniques of stabilization of Q- point in a transistor. *(Nov,09; May,13)*

16. The fixed bias circuit as shown in figure is subjected to an increase in junction temperature from 25°C to 75°C. If β is 125 at 75°C, determine the percentage change in Q point values (V_{CE}, I_C) over temperature change. Neglect any change in V_{BE}.
17. A self bias circuit has R_E=1 kΩ, R_1=130 kΩ, R_2=10 kΩ. If V_{CC} and R_C are adjusted to give I_C=1mA at 10°C. Calculate the variation in Ic over temperature change of 10°C to 100°C. The transistor used has the parameters given below,

Parameters	10°C	100°C
Ico (μA)	0.01	1.2
V_{BE}(V)	0.74	0.54
β	60	140

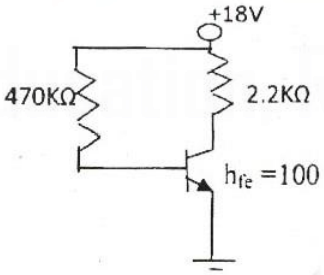
18. Design a collector to base bias circuit to have operating point (10v, 4mA). The circuit is supplied with 20v and uses a silicon transistor of hfe is 250.
19. Design a voltage divider bias circuit for the specified conditions. V_{CC}=12v, V_{CE}=6v, I_C=1mA, S=20, β=100 and V_E=1v.
20. The parameters for each transistor in the circuit in figure, are h_{fe} = 100, and $V_{BE(on)}$ = 0.7V. Determine the Q-point values of base collector and emitter currents in Q_1 and Q_2

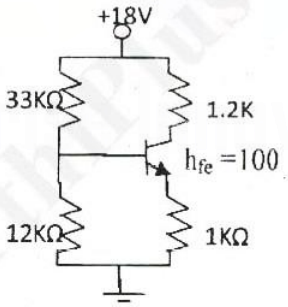
(8)[AU, MAY,2015]



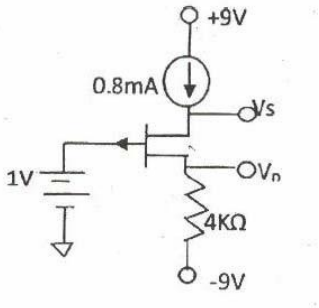
21. Determine the change in collector current produced in each bias referred to in fig 1 and 2, when the circuit temperature raised from 25°C to 105°C and I_{CBO} = 15nA @ 25°C

(8)[AU, MAY,2015]





22. Determine the quiescent current and voltage values in a P-Channel JFET circuit shown in fig. (8)[AU, MAY,2015]



23. The circuit shown in Fig, let h_{fe} = 100, (1). Find V_{TH} and R_{TH} for the base circuit. (2). Determine I_{CEQ} and V_{CEQ}. (3). Draw the DC load line. (8)[AU, MAY,2015]